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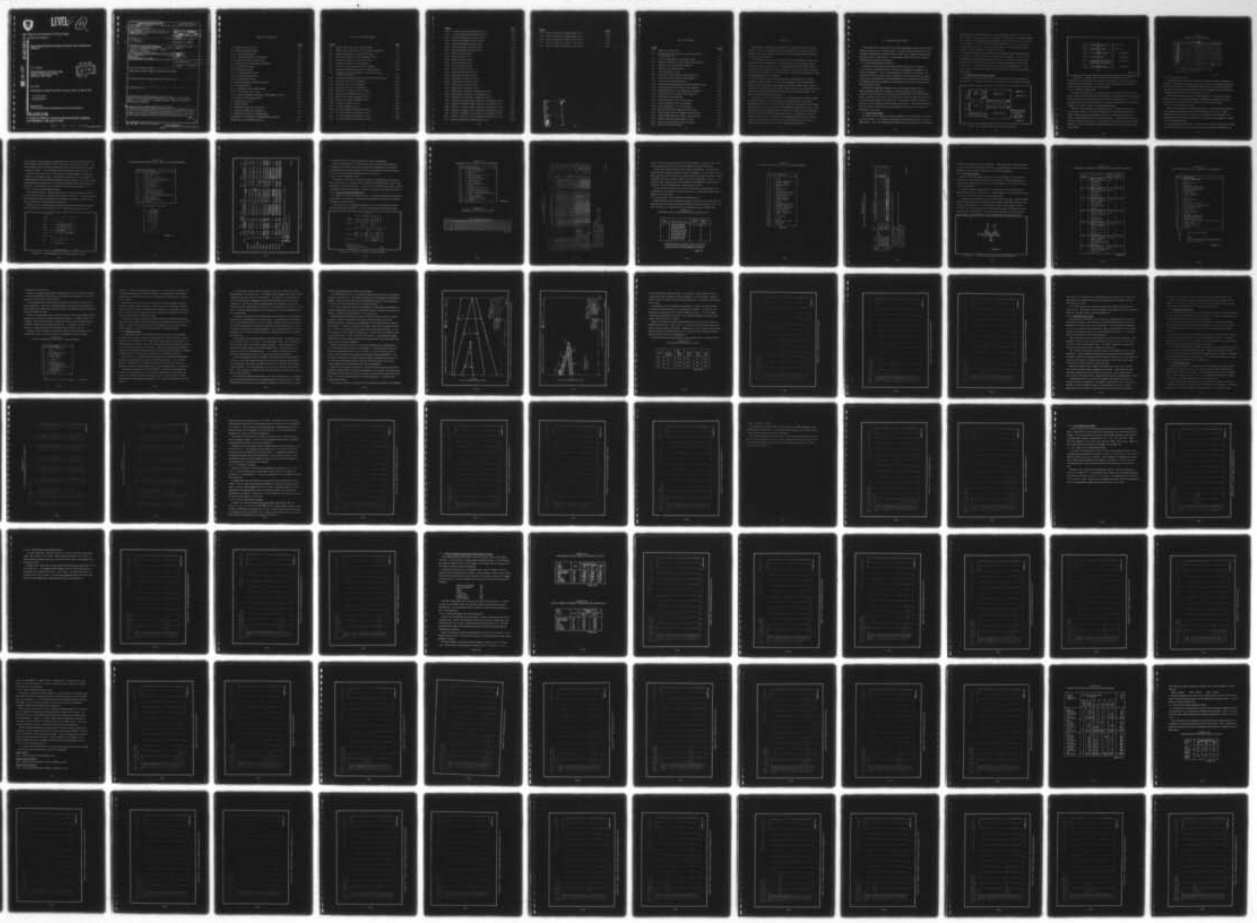

LEVEL II

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Research and Development Technical Report

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MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A manufacturing methods project has been initiated to establish a pilot production line for metal nitride oxide semiconductor (MNOS) block oriented random access memory (BORAM) multichip hybrid circuits. This report presents some measured characteristics of the BORAM 6002 chip.

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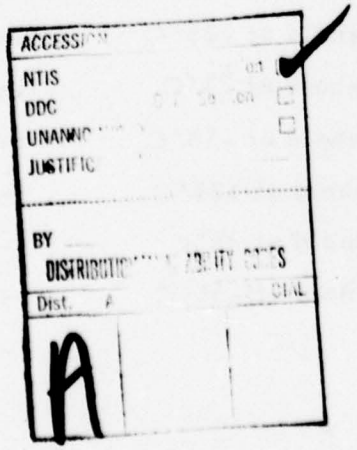

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PURPOSE

The purpose of manufacturing methods and technology (MM&T) project number 2769758 is to establish a production capability for metal-nitride-oxide semiconductor (MNOS) integrated circuits for block-oriented random-access memory (BORAM).

Military organizations are faced with a difficult hardware problem in the use of modern day computers. A suitable militarized secondary storage technology simply does not exist. Drums and discs cannot stand up under the stress of the ground mobile environment. Military real time programs are forced to be resident in main memory because electromechanical storage access delays cannot be tolerated.

MNOS BORAM holds considerable promise of meeting the military's secondary storage needs. An advanced development Army/Navy MNOS BORAM module has proven that significant volume, weight, power and use flexibility advantages can be achieved. When compared to fixed-head electro-mechanical storage MNOS BORAM offers MTBF's 10 times longer, and access times above 500 times faster.

This MM&T project will establish for the government a source of supply for MNOS BORAM secondary storage. A pilot production line with a demonstrated capacity of 1,875 hybrid circuit per month will be established. Each hybrid circuit will contain 16 MNOS BORAM integrated circuits. This production rate will provide sufficient hybrid circuits to allow fabrication of three 16.8 megabit BORAM modules per month. The hybrid circuits will conform to Electronics Command Technical Requirement SCS503, and the MM&T project will be conducted in accord with Electronics Command Industrial Preparedness Procurement Requirement Number 15.

1. NARRATIVE AND DATA

The BORAM 6002 integrated circuit is the development vehicle for the MNOS BORAM manufacturing methods project. During the reporting period the test capability developed for the pilot line was used to learn whether devices meet the specification of this program. This report reviews the status of the test capability and presents test results.

1.1 CHARACTERIZATION PROJECT

The devices manufactured during this MM&T project must conform to Army technical requirement SCS-503 which is presented as Appendix A for reference purposes. Prior to beginning pilot production it is necessary to interpret SCS-503 in terms of firm acceptance criteria for electrical screens. In the case of MNOS BORAM, this development was complicated by the need for defining tests which properly evaluate some of the unique characteristics associated with MNOS.

The technical approach employed was to first define specific tests to meet identified screening objectives. Then an automatic equipment test program was developed for the purpose of gathering data on the BORAM 6002 which could verify the validity of the tests and provide distribution information to allow setting suitable screening limits. The quantity of data involved required the use of computer data analysis and reduction. This information base was then used to define automatic test equipment screens for both wafer test and hybrid cricuit test.

1.1.1 Device Description

The 6002 chip is a 2048-bit memory intented for use in computer secondary storage systems. It is normally packaged in multichip hybrid form to achieve high density. Use of the MNOS (metal-oxide-nitride-semiconductor) technology

allows nonvolatile information storage and low power operation. The circuit design uses p-channel metal gate transistors on bulk silicon. All bonding pads are 5 mils^2, and are positioned on opposite side of the die for efficient hybrid circuit layout. A glass overcoat guards against scratches due to handling. All inputs have protective voltage limiting devices to avoid damage by static charge. The die measures 99 mils by 128 mils.

As shown in figure 1-1 the BORAM 6002 contains a fully decoded 64-word by 32-bit RAM and 32-bit dynamic two-phase shift register. All I/O are accomplished serially through the shift register. Parallel bidirectional data transfer between the RAM and the shift register takes place via an internal 32-bit latch. The RAM and shift register can operate independently. Data stored in the latch may be written into the RAM while new data is shifted into the register.

1.1.2 Characterization Test Program

Characterization of BORAM 6002 devices was aided by a Macrodata 501 test program. As shown in figure 1-2 six categories of tests were employed.

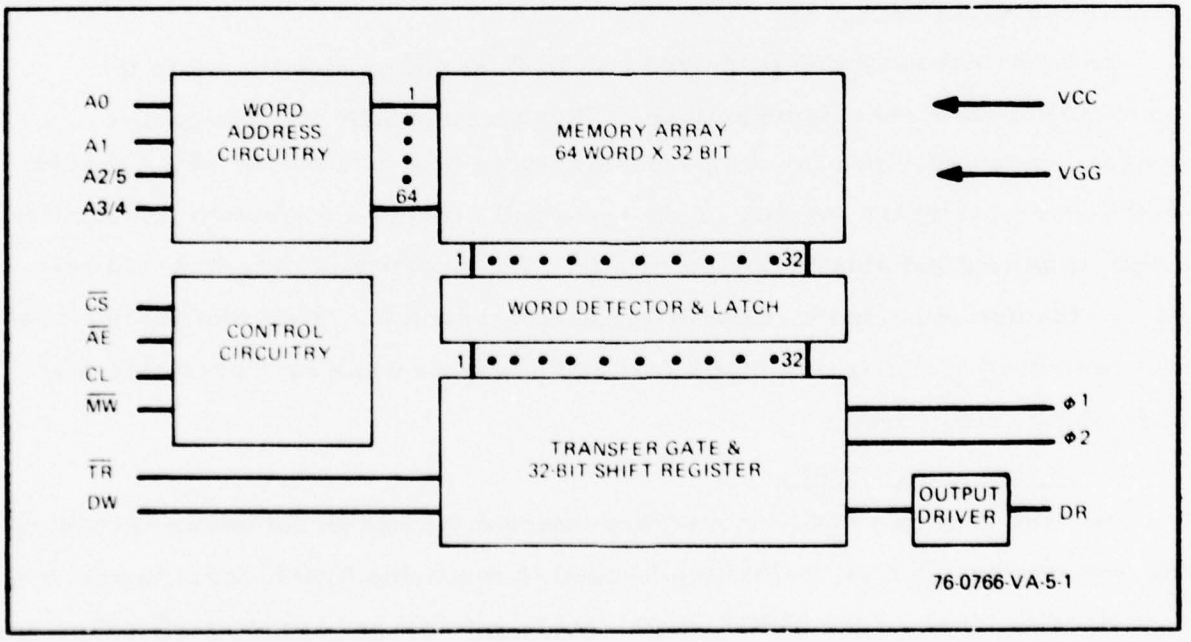

Figure 1-1. BORAM 6002 Functional Block Diagram

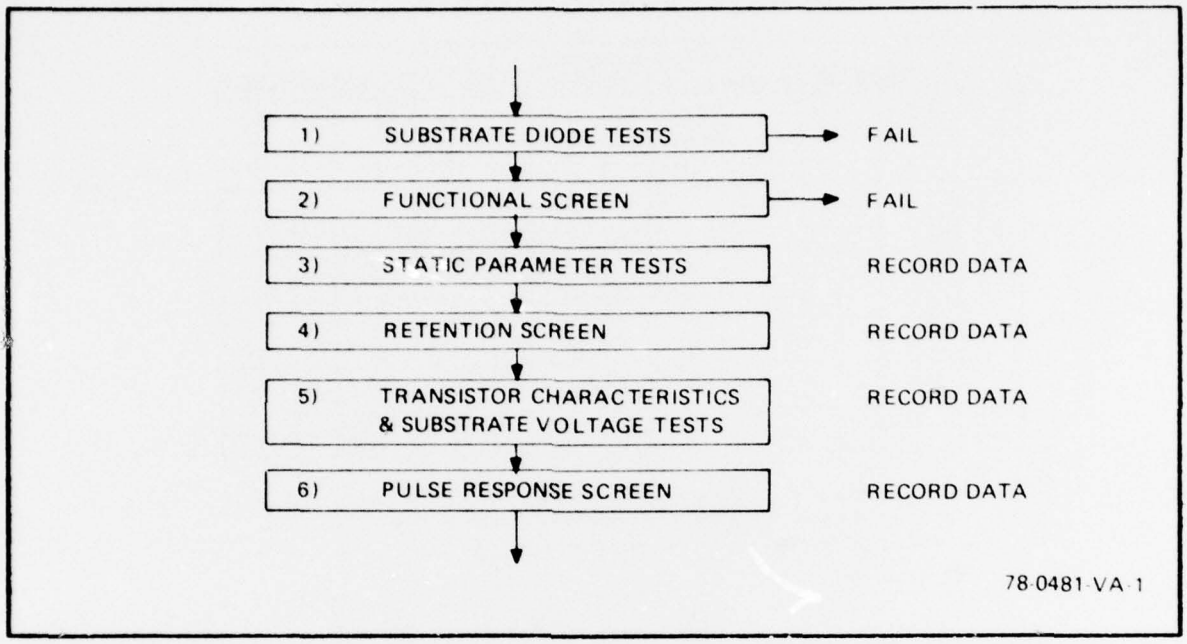

Figure 1-2. BORAM 6002 Electrical Test Functional Categories

The purpose of the program was to gather information on the nature of parts suitable for use in systems. The first two test categories were included to exclude nonfunctional parts from the data base.

1.1.2.1 Substrate Diode Tests

The substrate diode tests are relevant when the product is tested in wafer form. Observation of the forward voltage drop of the substrate diode associated with input terminals provides positive evidence of good probe contact. In rare cases this test can also be an indicator of process problems such as inadequate etching, poor ohmic contact, or improper diffusions.

Table 1-1 and associated foot notes define the 16 substrate diode tests. Every input terminal to the BORAM chip has an associated substrate diode. Under normal operating conditions where VCC is maintained as the most positive chip voltage this diode is reverse biased. A similar situation exists for the on-chip test structures. In this case the reference node is SUB rather than VCC. The GT terminal is isolated and does not have an associated substrate diode.

TABLE 1-1
SUBSTRATE DIODE TESTS

Test Number	Device Terminal Conditions[3]																			
	VCC	$\overline{TR}$	VGG	$\overline{CS}$	A2/5	A3/4	A0	A1	$\overline{AE}$	$\overline{MW}$	CL	DR	DW	ϕ2	ϕ1	SUB	MD	FD	GT[2]
1 1	GND	1																	
1 2	GND						1												
1 3	GND					1													
1 4	GND										1								
1 5	GND							1											
1 6	GND			1															
1 7	GND													1					
1 8	GND												1						
1 9	GND		1																
1 10	GND				1														
1 11	GND								1										
1 12	GND									1									
1 13	GND														1				
1 14	GND											1							
1 15																GND	1		
1 16																GND		1	

Notes

1. This is the node under test. Force 0.2 milliamperes into the node and measure the resulting voltage from the node to ground. Accept voltage readings from +0.3 volts up to 1.0volts.
2. The GT terminal does not have an associated substrate diode.
3. Terminals not labled are open circuited.

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1. 1. 2. 2 Functional Screen

The purpose of the functional screen is to quickly eliminate nonoperative die from consideration for characterization. Table 1-2 provides on overview of the six tests which are performed at nominal device operating conditions. This table references additional figures and tables which fully define the test conditions (figures 1-3 to 1-6 and tables 1-3 to 1-6).

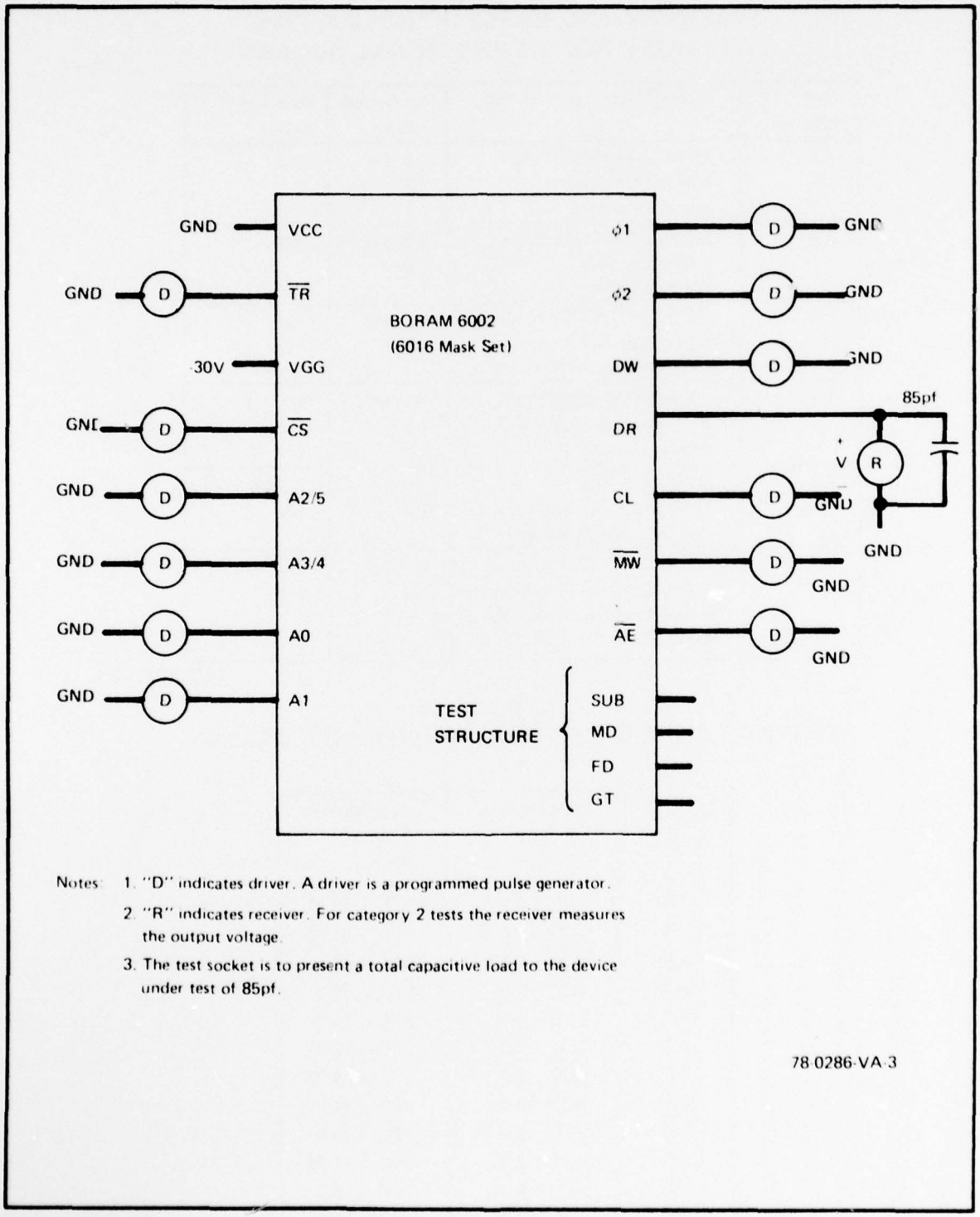
The first three tests exercise the shift register. The next test verifies that all memory cells can be properly addressed for writing and reading. The final two tests exercise all memory cells in both data states.

1. 1. 2. 3 Static Parameter Tests

Table 1-7 defines the static parameter tests. This test sequence exhaustively examines the device under test for leakage current levels, signal threshold values, output drive capability and supply current demand. The significance of these tests is examined in more detail in paragraph 1. 3 below.

1. 1. 2. 4 Retention Screen

The retention characteristics of a device are not directly measurable within the milliseconds of time that are practical for an automatic equipment test.



Notes:
1. "D" indicates driver. A driver is a programmed pulse generator.
2. "R" indicates receiver. For category 2 tests the receiver measures the output voltage.
3. The test socket is to present a total capacitive load to the device under test of 85pf.

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Figure 1-3. Signal Assignments for Functional Tests

TABLE 1-2
SUMMARY AND DESCRIPTION OF TEST
CATEGORY NO. 2 FUNCTIONAL SCREEN

Test Number	General Description of Test	Referenced Figures	Referenced Tables
2-1	SHIFT REGISTER TEST 1 MHz data rate zero data pattern	1-3, 1-4, 1-6	1-3
2-2	SHIFT REGISTER TEST 1 MHz data rate one data pattern	1-3, 1-4, 1-6	1-3
2-3	SHIFT REGISTER TEST 1 MHz data rate zero-one data pattern	1-3, 1-4, 1-6	1-3
2-4	ADDRESS & MEMORY TEST 1000μsec erase, 200μsec write diagonal data pattern	1-3, 1-5, 1-6	1-3, 1-4
2-5	MEMORY TEST 1000μsec erase, 200μsec write checkerboard data pattern	1-3, 1-5, 1-6	1-3,1-5, 1-6
2-6	MEMORY TEST 1000μsec erase, 200μsec write complementary checkerboard data pattern	1-3, 1-5, 1-6	1-3, 1-5, 1-6

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TABLE 1-3
DRIVER AMPLITUDES FOR FUNCTIONAL TESTS

Signal Symbol	Most Positive Amplitude Volts	Most Negative Amplitude Volts
$\overline{TR}$	VCC – 2.0	VCC – 10.5
$\overline{CS}$	VCC – 2.0	VCC – 34.65
A2/5	VCC – 2.0	VCC – 10.5
A3/4	VCC – 2.0	VCC – 10.5
A0	VCC – 2.0	VCC – 10.5
A1	VCC – 2.0	VCC – 10.5
ϕ1	VCC – 2.0	VCC – 14.25
ϕ2	VCC – 2.0	VCC – 14.25
DW	VCC – 2.0	VCC – 10.5
CL	VCC – 2.0	VCC – 14.25
$\overline{MW}$	VCC – 2.0	VCC – 10.5
$\overline{AE}$	VCC – 2.0	VCC – 10.5

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The objective of the retention oriented test in the characterization program was to isolate chips which are likely to have poor nonvolatile retention. The test simulates end-of-retention conditions by writing the memory cells using a reduced voltage. Test conditions are documented in tables 1-8 and 1-9.

Note that erase and read are performed at nominal supply voltages and nominal control signal timing. This avoids confusion of circuit voltage and timing operating limitations with possible retention defects. The write voltage is progressively reduced until the threshold voltage window can no longer be detected. The interpretation of this test is discussed in paragraph 1. 2. 2.

1. 1. 2. 5 Test Structure Measurements

The BORAM 6002 die contains some device structures which are not part of the functional memory configuration defined in figure 1-1. These structures were provided to allow measurement of fundamental process characteristics, and include several capacitors and transistors.

Probe test is a convenient point to gather statistically significant amounts of data without incurring excessive cost. These test structures are not

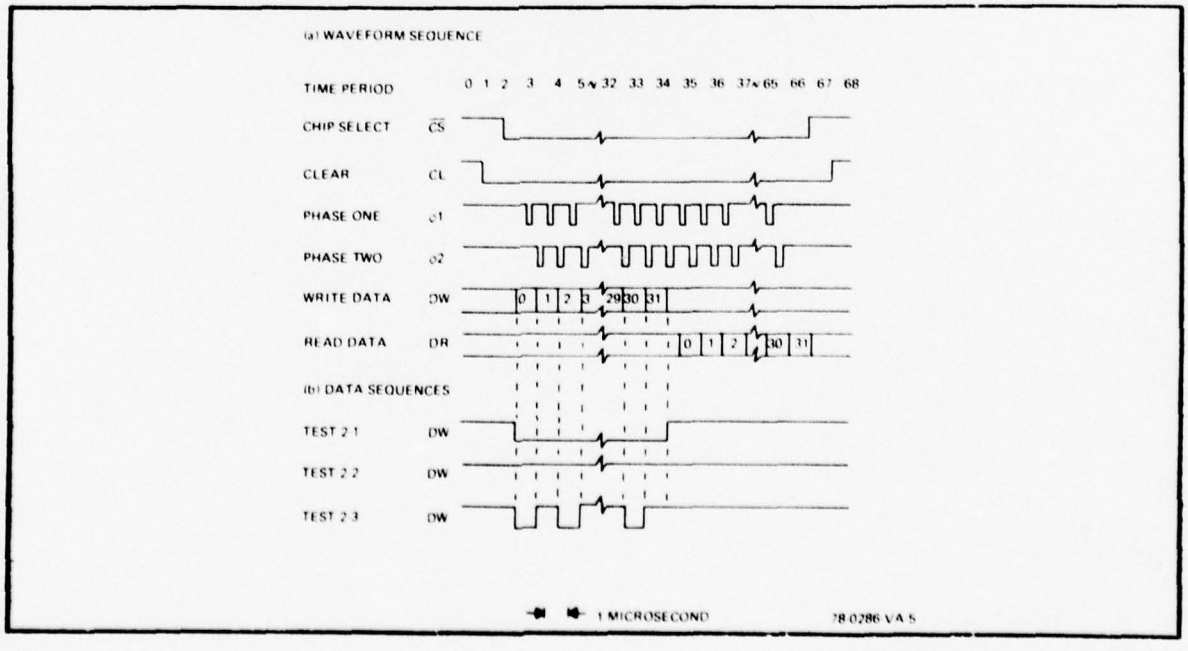

Figure 1-4. Operating Sequence for Shift Register Tests

TABLE 1-4
ADDRESS AND MEMORY TEST LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 5a
2	Block Erase per Fig. 5b
3	Address = 0
4	Setup Address Lines per Fig. 5c
5	Data = Function (Address) per Note Below
6	Load Shift Register per Fig. 5d
7	Write Data per Fig. 5e
8	Address = Address + 1
9	If (Address < 64) then 4
10	Address = 0
11	Setup Address Lines per Fig. 5c
12	Read Data to Latch per Fig. 5f
13	Empty Shift Register per Fig. 5g
14	If (Data ≠ Function (Address)) then BIN and 18
15	Address = Address + 1
16	If (Address < 64) then 11
17	Reset CS and CL per Fig. 5h
18	End Routine

Note: Diagonal Data Pattern per Figure below:

	Columns					
Rows	0	1	~	30	31	
0	0	0	0	0	0	1
1	0	0	0	0	1	0
⎫	0	0	0	1	0	0
⎭	0	0	1	0	0	0
30	0	1	0	0	0	0
31	1	0	0	0	0	0
32	1	1	1	1	1	0
33	1	1	1	1	0	1
⎫	1	1	1	0	1	1
⎭	1	1	0	1	1	1
62	1	0	1	1	1	1
63	0	1	1	1	1	1

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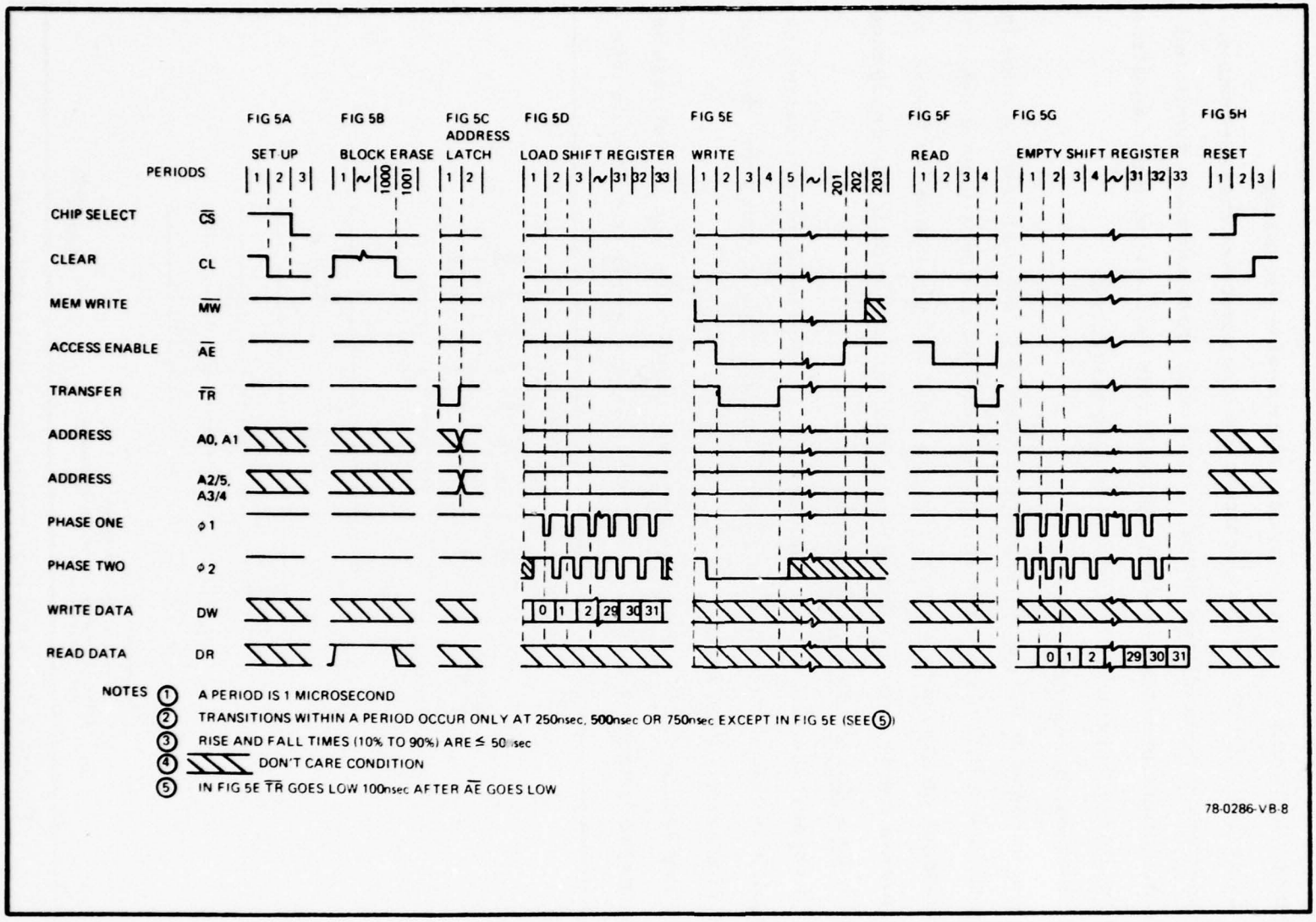

Figure 1-5. Operating Sequences for Memory Tests

normally available for measurements after device packaging.

Table 1-10 and figure 1-7 document the test structure measurements. Nonmemory threshold, and memory transistor thresholds are monitored. The magnitude of voltage present on the N type epitaxial memory substrate for two circuit operating conditions is also measured.

1.1.2.6 Pulse Response Screen

The purpose of the pulse response screen is to exhaustively examine the part to insure that it can perform in all operating modes without a detracting dependence on past data history. Tables 1-11 to 1-14 define the tests. Figure 8 presents the waveform sequence required for operation in the group mode.

1.1.3 Data Collection and Reduction

To support the characterization project a computer program was prepared to facilitate the collection, organization and analysis of data from the Macrodata characterization tests.

A key feature of this computer program is the collection of test results on a magnetic tape cartridge. Data for individual parts is stored on tape

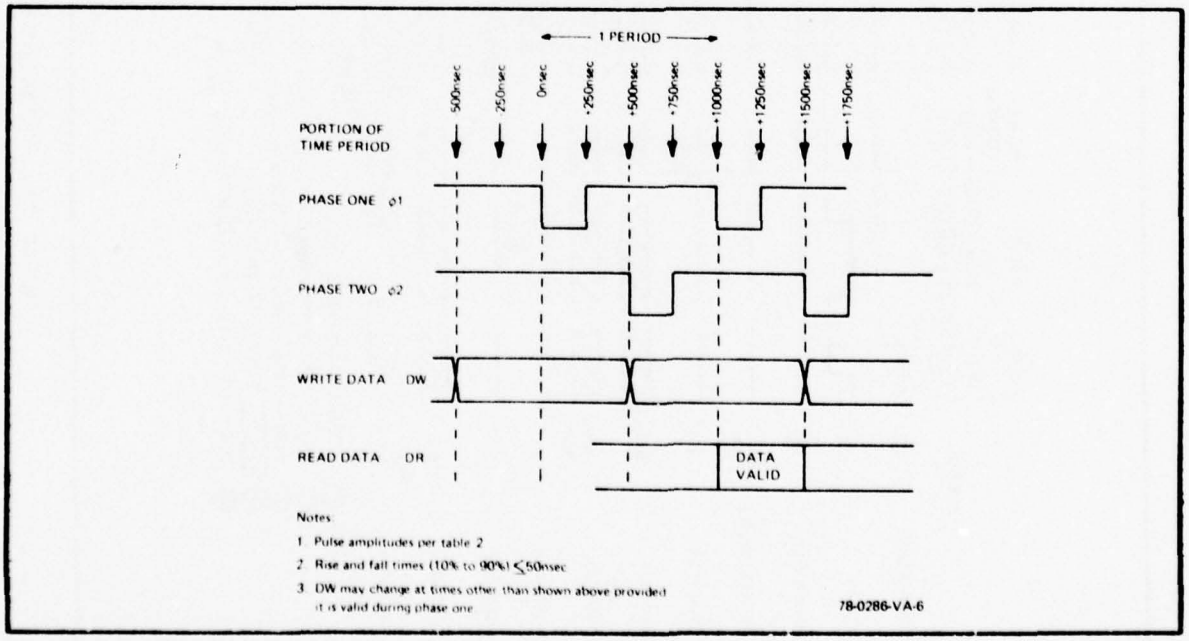

Figure 1-6. Detailed Timing for Clocks and Data

TABLE 1-5
MEMORY TEST LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 5a
2	Block Erase per Fig. 5b
3	Address = 0
4	Setup Address Lines per Fig. 5c
5	Data = (per Table 6)
6	Load Shift Register per Fig. 5d
7	Write Data per Fig. 5e
8	Address = Address + 1
9	If (Address < 64) then 4
10	Address = 0
11	Setup Address Lines per Fig. 5c
12	Read Data to Latch per Fig. 5f
13	Empty Shift Register per Fig. 5g
14	If (Data ≠ (per Table 6)) then BIN and 18
15	Address = Address + 1
16	If (Address < 64) then 11
17	Reset $\overline{CS}$ and CL per Fig. 5h
18	End Routine

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TABLE 1-6
MEMORY TEST DATA PATTERNS

Test Number	Row Address	Data Pattern Required In Shift Register																													
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2-5	Even	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
2-5	Odd	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2-6	Even	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
2-6	Odd	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

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TABLE 1-7
STATIC PARAMETER TESTS

Test Number	Test Description	Device Terminal Conditions [6]															Terminal Under Test	25°C Test Limits		
		VCC	$\overline{TR}$	VGG	$\overline{CS}$	A2/5	A3/4	A0	A1	$\overline{AE}$	$\overline{MW}$	CL	DR	DW	ϕ2	ϕ1		Min	Max	Units
3-1	Input Leakage	1			-37.5V												$\overline{CS}$		2.0	µA
3-2	Input Leakage	+20V	2	-10V	+20V	+20V	+20V	+20V	+20V	+20V	+20V	+5V		+20V	+20V	+20V	$\overline{TR}$		1.0	µA
3-3	Input Leakage	+20V	+20V	-10V	+20V	+20V	+20V	2	+20V	+20V	+20V	+5V		+20V	+20V	+20V	A0		1.0	µA
3-4	Input Leakage	+20V	+20V	-10V	+20V	+20V	2	+20V	+20V	+20V	+20V	+5V		+20V	+20V	+20V	A3/4		1.0	µA
3-5	Input Leakage	+20V	+20V	-10V	+20V	+20V	+20V	+20V	2	+20V	+20V	+5V		+20V	+20V	+20V	A1		1.0	µA
3-6	Input Leakage	+20V	+20V	-10V	+20V	+20V	+20V	+20V	+20V	+20V	+20V	+5V		+20V	2	+20V	ϕ2		1.0	µA
3-7	Input Leakage	+20V	+20V	-10V	+20V	+20V	+20V	+20V	+20V	+20V	+20V	+5V		2	+20V	+20V	DW		1.0	µA
3-8	Input Leakage	+20V	+20V	-10V	+20V	2	+20V	+20V	+20V	+20V	+20V	+5V		+20V	+20V	+20V	A2/5		1.0	µA
3-9	Input Leakage	+20V	+20V	-10V	+20V	+20V	+20V	+20V	+20V	2	+20V	+5V		+20V	+20V	+20V	$\overline{AE}$		1.0	µA
3-10	Input Leakage	+20V	+20V	-10V	+20V	+20V	+20V	+20V	+20V	+20V	2	+5V		+20V	+20V	+20V	$\overline{MW}$		1.0	µA
3-11	Input Leakage	+20V	+20V	-10V	+20V	+20V	+20V	+20V	+20V	+20V	+20V	+5V		+20V	+20V	2	ϕ1		1.0	µA
3-12	Tristate Leakage	+20V	+20V	-10V	+20V	+20V	+20V	+20V	+20V	+20V	+20V	+5V	2	+20V	+20V	+20V	DR		1.0	µA
3-13	Input & Output Low Voltage Test	GND	GND	-30V	-35V	GND	GND	GND	GND	GND	GND	-15V	3	-10.25V	-14V	-14V	DR	-10.5		Volts
3-14	Input & Output High Voltage Test	GND	GND	-30V	-35V	GND	GND	GND	GND	GND	GND	-15V	4	-1.75V	-14V	-14V	DR		4.5	Volts
3-15	Supply Current Deselected Standby	5	GND	-30V	GND	GND	GND	GND	GND	GND	GND	-15V		GND	GND	GND	VCC		100.0	µA
3-16	Supply Current Selected Standby	5	GND	-33V	-33V	GND	GND	GND	GND	GND	GND	-15V		GND	GND	GND	VCC	7.0	15.0	mA
3-17	Supply Current Read	5	GND	-33V	-33V	GND	GND	GND	GND	-15V	GND	-15V		GND	GND	GND	VCC	11.0	37.0	mA
3-18	Supply Current Write	5	GND	-33V	-33V	GND	GND	GND	GND	-15V	-15V	-15V		GND	GND	GND	VCC	10.0	32.0	mA
3-19	Supply Current - Chip Clear	5	GND	-33V	-33V	GND	GND	GND	GND	GND	GND	GND		GND	GND	GND	VCC	7.0	15.0	mA
3-20	Supply Current - Group Clear	5	GND	-33V	-33V	GND	GND	GND	GND	-15V	-15V	GND		GND	GND	GND	VCC	8.0	18.0	mA

Notes

1. Measure the current flow from GND into VCC
2. Measure the current flow out of this node to GND
3. Force 5 milliamperes into DR and measure the voltage from DR to GND
4. Force 5 milliamperes out of DR and measure the voltage from DR to GND
5. Measure the current from GND into VCC
6. Terminals not labled are open circuited

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files, and can be automatically searched and updated. Extensive user interaction features promote checking and comparison of stored results.

Two primary data summary features were established. The first was a statistical data summary report for specific samples. In this case the computer searches the tape files for all parts which meet some selection criteria. A possible selection criteria might be "all parts measured at +125°C." The program then computes means and measures of dispersion, and prints the results for the 26 variables data characterization tests.

The second data summary feature of the program is the preparation of histograms for individual characterization tests. Examples of these reports appear in the text below.

1.2 FUNCTIONAL TEST CONCEPTS AND RESULTS

MNOS BORAM devices necessarily have a great deal in common with conventional semiconductor memories and share similar problems in test. On the other hand, the nonvolatility and the physical nature of MNOS does

TABLE 1-8
SUMMARY AND DESCRIPTION OF RETENTION TEST

Test Number	General Description of Test	Referenced Figures	Referenced Tables
4-1	RETENTION SCREEN 1000μ sec erase, 200μ sec write all zero and all one data patterns VGG= –30 V for erase and read VGG for write is reduced by 0.5V increments until the device under test fails. The last pass voltage is recorded.	1-3*, 1-5, 1-6,	1-3, 1-9

* Provision must be made for varying VGG. In figure 1-3 VGG is shown as –30 volts. At the option of the test programmer a driver may be assigned to this terminal or the supply voltage may be incremented.

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TABLE 1-9
RETENTION SCREEN LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	J = −30
2	K = 0
3	Setup CL and $\overline{CS}$ per fig. 5a.
4	Set VGG = −30 volts
5	Block erase per fig. 5b
6	Data = K
7	Set VGG = J volts
8	Address = 0
9	Setup address lines per fig. 5c
10	Load shift register per fig. 5d
11	Write data per fig. 5e
12	Address = address +1
13	If (address < 64) then 9
14	Set VGG = −30 volts
15	Address = 0
16	Setup address lines per fig. 5c
17	Read data to latch per fig. 5f
18	Empty shift register per fig. 5g
19	If (data ≠ K) then 26
20	Address = address +1
21	If (address < 64) then 16
22	K = $\overline{K}$
23	If (K = 1) then 4
24	J = J + 0.5
25	Go to 4
26	Reset $\overline{CS}$ and CL per fig. 5h
27	Print J = 0.5
28	End Routine

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TABLE 1-10
TEST STRUCTURE MEASUREMENTS

Test Number	Description	Phase of test	Device Terminal Conditions																			
			VCC	$\overline{TR}$	VGG	$\overline{CS}$	A2/5	A3/4	A0	A1	$\overline{AE}$	$\overline{MW}$	CL	DR	DW	ø2	ø1	SUB	MD	FD	GT
5.1	Nonmemory threshold voltage	measurement																GND		1	1
5.2	Memory high conduction threshold voltage	set-up																GND			2
		measurement																GND	3		3
5.3	Memory low conduction threshold voltage	set-up																GND			4
		measurement																GND	3		3
5.4	Substrate voltage high	measurement	GND	GND	30V	35V	GND	GND	GND	GND	15V	GND	15V	GND	GND	GND	GND	5			
5.5	Substrate voltage low	measurement	GND	GND	30V	35V	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5			

Notes:

1. Tie the fixed drain (FD) and gate (GT) terminals together. Force 10 microamps out of the node and measure the voltage from the node to ground. (GND)
2. Pulse GT to +25 volts for 1 millisecond.
3. Tie the memory drain (MD) and gate (GT) terminals together. Force 10 microamps out of the node and measure the voltage from the node to ground. (GND)
4. Pulse GT to -25 volts for 200 microseconds.
5. Measure the voltage from SUB to (GND).

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introduce some new tests considerations. This discussion reviews the rational for each of the functionally oriented tests employed in the characterization program, and the results obtained from a sample population.

1.2.1 Functional Screen

Before considering a part suitable for characterization it is screened to certify that it does operate properly as a memory. The test approach first verifies shift register operation, and then continues to confirm that the RAM performs adequately.

The shift register is operated at a 1 MHz rate into a rated load with all input signals at worst rated values. The data pattern is varied from all zeros to all ones, and then to alternating zeros and ones.

The operation of the device as a BORAM is then examined. Address unique data (a diagonal pattern) is shifted into the register and written into the RAM. This is accomplished at a 1 MHz shift rate with all input signals at worst rated values. Rated erase time of 1000 microseconds and write time of 200 microseconds is employed. The entire chip is written, and then the entire chip is read. This procedure is then repeated using checkerboard and

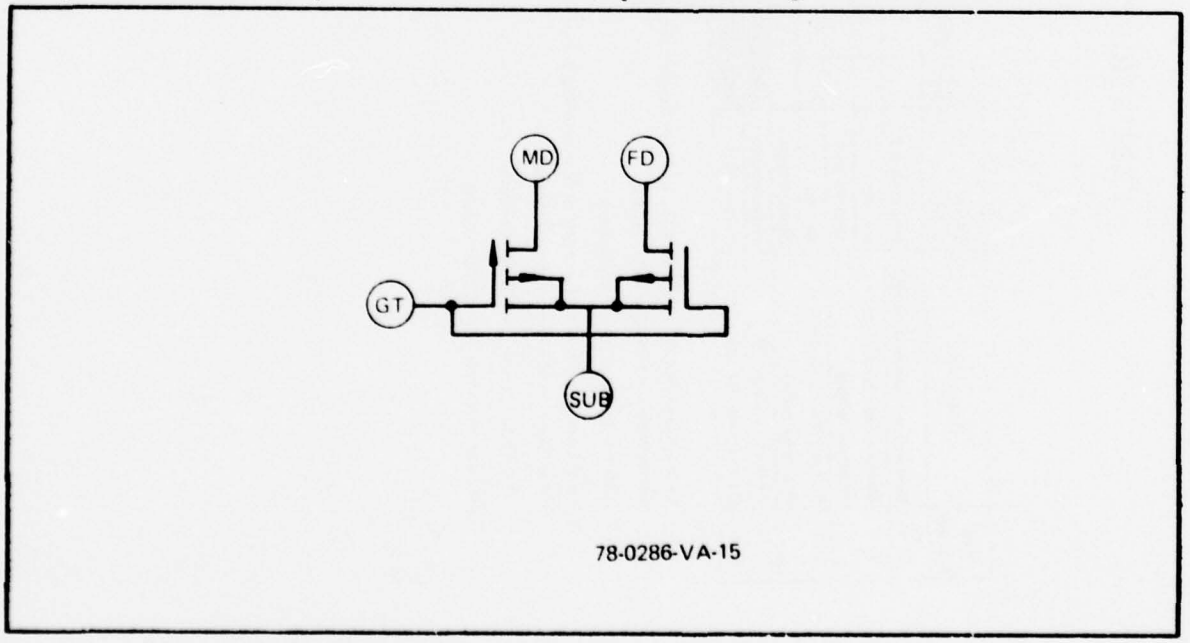

Figure 1-7. Transistor Test Structure Circuit Diagram

TABLE 1-11
SUMMARY AND DESCRIPTION OF PULSE RESPONSE SCREEN

Test Number	General Description of Test	Referenced Figures	Referenced Tables
6-1	ERASE RECOVERY TEST 1000μsec erase, 200μsec write zero data pattern erase-write 100 times one data pattern erase-write 1 time, read	1-3, 1-5, 1-6	1-3, 1-12
6-2	ERASE RECOVERY TEST 1000μsec erase, 200μsec write one data pattern erase-write 100 times zero data pattern erase-write 1 time, read	1-3, 1-5, 1-6	1-3, 1-12
6-3	ERASE RECOVERY TEST 1000μsec erase, 200μsec write checkerboard pattern erase-write 100 times complement checkerboard pattern erase-write 1 time, read	1-3, 1-5, 1-6	1-3, 1-12
6-4	ERASE RECOVERY TEST 1000μsec erase, 200μsec write complement checkerboard pattern erase-write 100 times checkerboard pattern erase-write 1 time, read	1-3, 1-5, 1-6	1-3, 1-12
6-5	GROUP OPERATION TEST 1000μsec erase, 200μsec write complement checkerboard pattern begin at address 63 and count down group erase-write entire chip read entire chip	1-3, 1-5, 1-6, 1-8	1-3, 1-13
6-6	GROUP OPERATION TEST 1000μsec erase, 200μsec write checkerboard pattern begin at address 0 and count up group erase-write entire chip read entire chip	1-3, 1-5, 1-6, 1-8	1-3, 1-13
6-7	READ DISTURB TEST use data written during test 6-6 read data to latch 1000 times read entire chip	1-3, 1-5, 1-6	1-3, 1-14

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TABLE 1-12
ERASE RECOVERY TEST LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 5a
2	J = 1
3	Block Erase per Fig. 5b
4	Address = 0
5	Setup Address Lines per Fig. 5c
6	Data = (per Note at Bottom of Page)
7	Load Shift Register per Fig. 5d
8	Write Data per Fig. 5e
9	Address = Address + 1
10	If (Address < 64) then 5
11	J = J + 1
12	If (J < 101) then 3
13	Block Erase per Fig. 5b
14	Address = 0
15	Setup Address Lines per Fig. 5c
16	Data = (Complement of Data used in Step 6)
17	Load Shift Register per Fig. 5d
18	Write Data per Fig. 5e
19	Address = Address + 1
20	If (Address < 64) then 15
21	Address = 0
22	Setup Address Lines per Fig. 5c
23	Read Data to Latch per Fig. 5f
24	Empty Shift Register per Fig. 5g
25	If (Data ≠ (Complement of Data used in Step 6)) then BIN and 29
26	Address = Address + 1
27	If (Address < 64) then 22
28	Reset $\overline{CS}$ and CL per Fig. 5h
29	End Routine

Note:

Test Number	Data Pattern to be Used in Step 6
6-1	All Zero
6-2	All One
6-3	Checkerboard (Defined in Table 1-6 for Test Number 2-5)
6-4	Complement Checkerboard

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TABLE 1-13
GROUP OPERATION'S TEST LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 5a
2	Address = (63 for Test 6-5) (0 for Test 6-6)
3	Setup Address Lines per Fig. 5c
4	Group Erase per Fig. 8
5	Data (per Note at Bottom of Page)
6	Load Shift Register per Fig. 5d
7	Write Data per Fig. 5e
8	Address = (Address - 1 for Test 6-5) (Address + 1 for Test 6-6)
9	Load Shift Register per Fig. 5d
10	Write Data per Fig. 5e
11	Address = (Address - 1 for Test 6-5) (Address + 1 for Test 6-6)
12	Load Shift Register per Fig. 5d
13	Write Data per Fig. 5e
14	Address = (Address - 1 for Test 6-5) (Address + 1 for Test 6-6)
15	Load Shift Register per Fig. 5d
16	Write Data per Fig. 5e
17	Address = (Address - 1 for Test 6-5) (Address + 1 for Test 6-6)
18	(If Address ≠ -1 then 3 for Test 6-5) (If Address ≠ 64 then 3 for Test 6-6)
19	Address = 0
20	Setup Address Lines per Fig. 5c
21	Read Data to Latch per Fig. 5f
22	Empty Shift Register per Fig. 5g
23	If Data ≠ (per Note at Bottom of Page) then BIN and 26
24	Address = Address + 1
25	If Address ≠ 64 then 20
26	Reset $\overline{CS}$ and CL per Fig. 5h
27	End Routine

Note

Test Number	Data Pattern
6-5	Complement Checkerboard
6-6	Checkerboard (Defined in Table 1-6 for Test Number 2-5)

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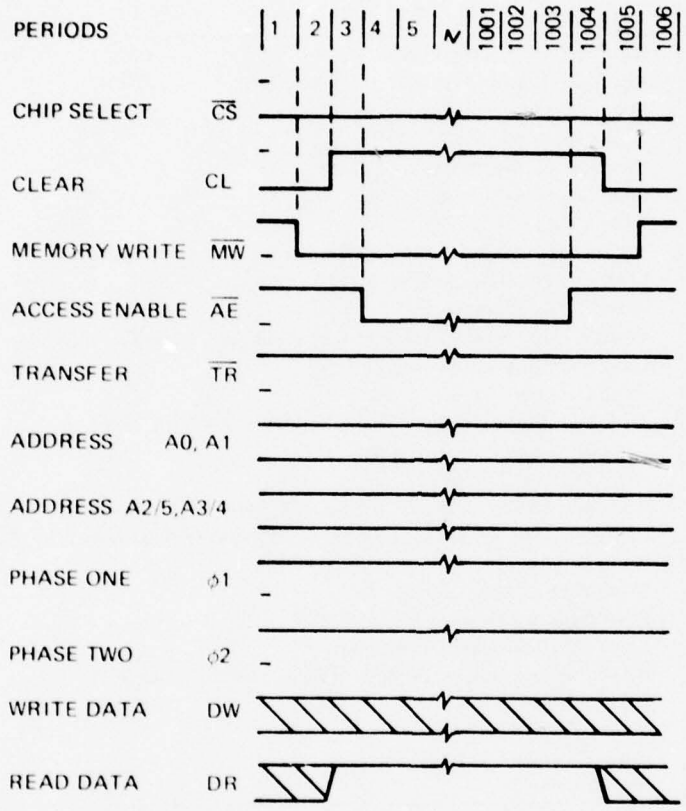

NOTES:
1. A period is 1 microsecond.
2. No transitions occur within a period.
3. Rise and fall times (10% to 90%) $\leq$ 50ns
4. ▨ don't care condition.

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Figure 1-8. Operating Waveform Sequence for Group Erase

checkerboard bar patterns.

The use of address unique data verified that every cell could be accessed. The use of the additional data patterns eliminated the possibility of hard cell (stuck at one or stuck at zero) failures.

This straightforward test sequence provides a first order verification of device operation. The use of a limited number of data patterns is believed to be adequate for MNOS type devices because the classical problem of pattern sensitivity does not exist.

Volatile semiconductor memories have in some cases been found to operate improperly as a function of particular data patterns. In dynamic RAM's for example, data stored as charge on capacitive nodes can be disturbed by the transient conditions surrounding a given cell. Transients can also act to disturb the proper operation of other parts of the memory circuit.

Complex three dimensional *distributed* capacative networks exist within these chips, and it is difficult to predict all possible modes of charge

TABLE 1-14
READ DISTURB TEST LOGICAL FLOW SEQUENCE

Step	Logical Operation
1	Setup CL and $\overline{CS}$ per Fig. 5a
2	J = 1
3	Address = 0
4	Setup Address Lines per Fig. 5c
5	Read Data to Latch per Fig. 5f
6	Address = Address + 1
7	If (Address < 64) then 4
8	J = J + 1
9	If (J < 1001) then 3
10	Address = 0
11	Setup Address Lines per Fig. 5c
12	Read Data to Latch per Fig. 5f
13	Empty Shift Register per Fig. 5g
14	If (Data ≠ Checkerboard) then BIN and 18
15	Address = Address + 1
16	If (Address < 64) then 11
17	Reset $\overline{CS}$ and CL per Fig. 5h
18	End Routine

Note
Checkerboard Pattern Defined in Table 1-6 for Test Number 25

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transfer. From a test standpoint attempts are made to cause changes in cell data in the presence of all possible adjacent cell conditions. Many subtle situations can exist within an array, and exhaustive testing is not economically feasible.

MNOS memory devices store information as charge trapped within the memory transistor gate insulator. This charge is very difficult to disturb as a function of normal circuit operating transients. The storage cell is in effect immune from the classical pattern sensitivity mechanism associated with charge storage on capacitive nodes.

Freedom from pattern sensitivity effects has been examined by exploratory tests with a wide variety of data patterns conducted at the Naval Air Test Center. Devices in a BORAM advanced development unit were exercised under computer control with no observed pattern related failures.

1.2.2 Retention Screen

The nonvolatile nature of MNOS memory poses a special test problem. Examination of memory transistor threshold decay characteristics, and experience with BORAM devices, leads to the expectation of several years of unpowered data retention. Since the beginning of BORAM development efforts the retention goal has been 4,000 hours. The testing problem boils down to finding some meaningful measurement performed in milliseconds on automatic equipment which can predict performance over a 4,000-hour period.

Researchers at Westinghouse and elsewhere have examined this problem and have proposed different approaches which have merit. The utility of specific techniques must be judged in the context of the device involved. Economic objectives, packaging and part circuit design must be considered.

The approach used for the BORAM 6002 is to screen for homogeneous memory cell characteristics. The implicit assumption is that defect free devices are capable of meeting retention goals. If a given device differs significantly from the parent population, it is viewed as a potential retention failure.

To communicate clearly the test rational it is first necessary to outline the operation of a memory cell. The BORAM 6002 employs two MNOS memory transistors to store one bit of information. The detection of stored data involves a differential comparison of the threshold voltage states of the two transistors. Storage of a ONE is defined when one transistor is in a high conduction (VHC) state and the other is in a low conduction (VLC) state. Storage of a ZERO is defined when the two transistors are in states opposite that for a stored ONE.

In a defect free device the threshold difference between the two transistors is quite large immediately after data storage. As time goes by, both transistor thresholds decay slowly in such a manner that the difference decreases. The end of retention occurs when the difference becomes so small it can not be reliably detected by the sense amplifier. The retention period for a device depends on the size of the initial difference (window) and the rate of decay of the difference.

The process of storing information involves two steps. The initial operation is called "clear" or "erase". Both transistors in the cell are subjected to a 1 millisecond +25 volt gate to substrate pulse. Both transistors are shifted to the high conduction (VHC) threshold state. In this case the cell does not contain any meaningful data. . . . i. e. when both transistors are in the high conduction state the cell content is logically indeterminate.

The second operation called "writing" acts to shift one of the transistors in the cell to the low conduction state as a function of the data input signal. The transistor to be written is subjected to a -25 volt 200 microsecond gate to source pulse. After this operation the cell is in a logically determinate state. One transistor remains in the cleared condition, and the other transistor has been written.

The threshold voltage window between the two transistors in a cell depends on the amplitude and duration of the pulses used for erase and write. Small windows which simulate end-of-retention conditions can be achieved by using

smaller amplitudes and/or shorter pulsewidths.

In a BORAM 6002 device, the option of using narrow erase or write pulsewidths is not practical. The memory transistor will respond to microsecond pulses. This time is so short that the propagation delays in the peripheral on-chip circuitry would dominate circuit performance.

The choice of end-of-retention simulation by reduced pulse amplitudes is easily accomplished, and can be performed in such a manner as to avoid confusing cell operation and peripheral circuit operation.

Experiments with individual memory transistors illustrate the concepts involved. Figure 1-9 shows how the decay characteristic curves for a BORAM transistor change as the amplitudes of the erase and write voltages are changed. At reduced voltages the window closes up in a predictable manner. At ±25 volts the projected window closure point was off scale. At ±23 volts closure occurs at about 10,000 hours. For ±21 volts the window closes in less than 1 hour. This of course is no surprise. The threshold voltage shift achieved at any given erase and write pulsewidth is directly proportional to the erase and write amplitude.

Figure 1-10 illustrates how a reduced threshold window established by a ±21 volt pulse could be used to screen product. In this experiment five devices were observed at the ±21 volt condition. Four of the devices were known to have characteristics typical of the parent device population. The fifth device was known to exhibit nontypical pulse response characteristics. If a test were performed using a 30 second read delay time, the maveric sample could be distinguished from the typical population.

This then is the general concept for a screen to detect memory cells with potential retention (and/or endurance) problems. One further refinement was introduced to make the screen more relevant to actual device operating conditions. The erase voltage was held at nominal amplitude. Only the write voltage was reduced.

The normal condition for writing is for the memory transistor to be initially

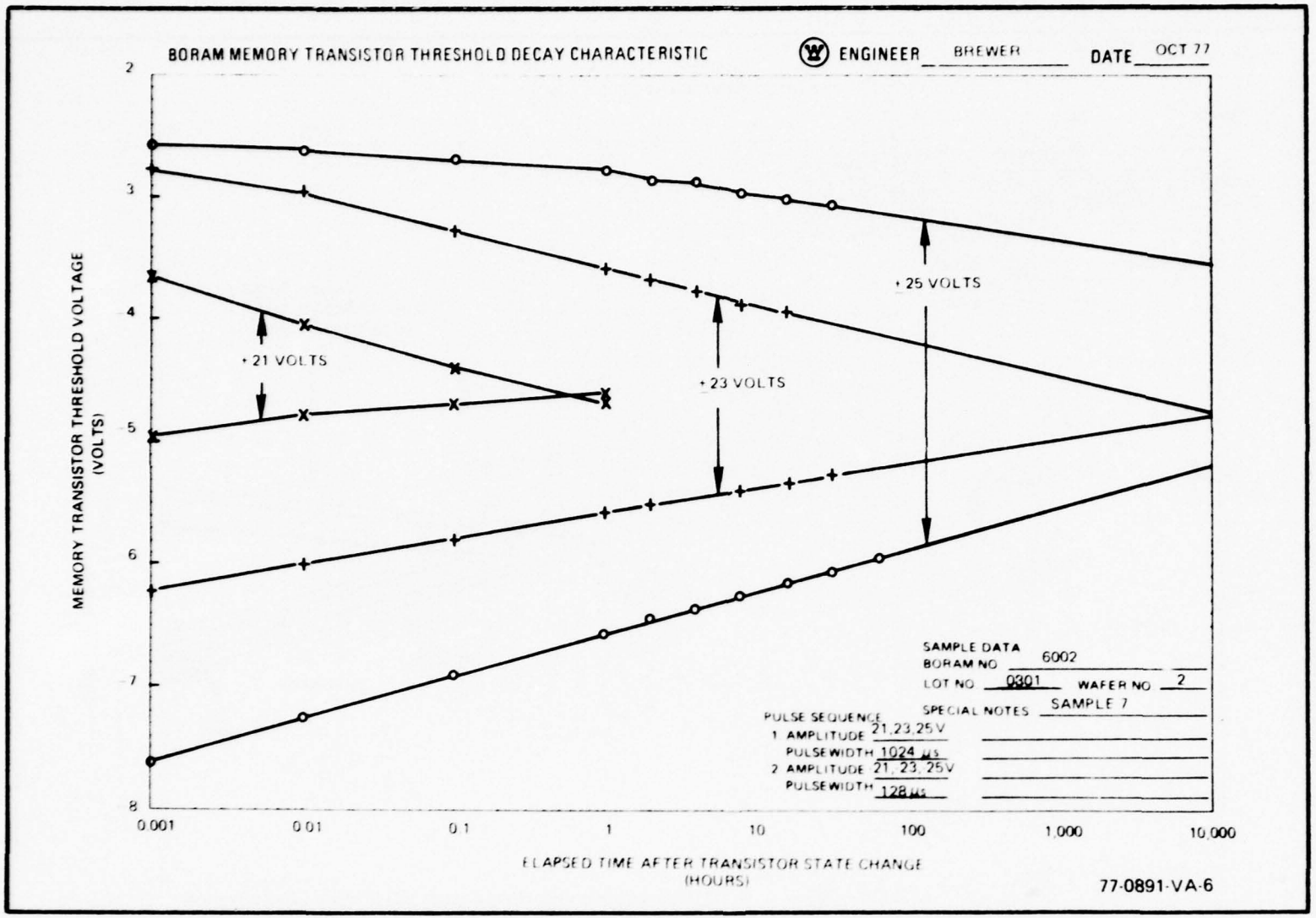

Figure 1-9. Threshold Voltage Window for Three Write/Erase Voltage Amplitudes

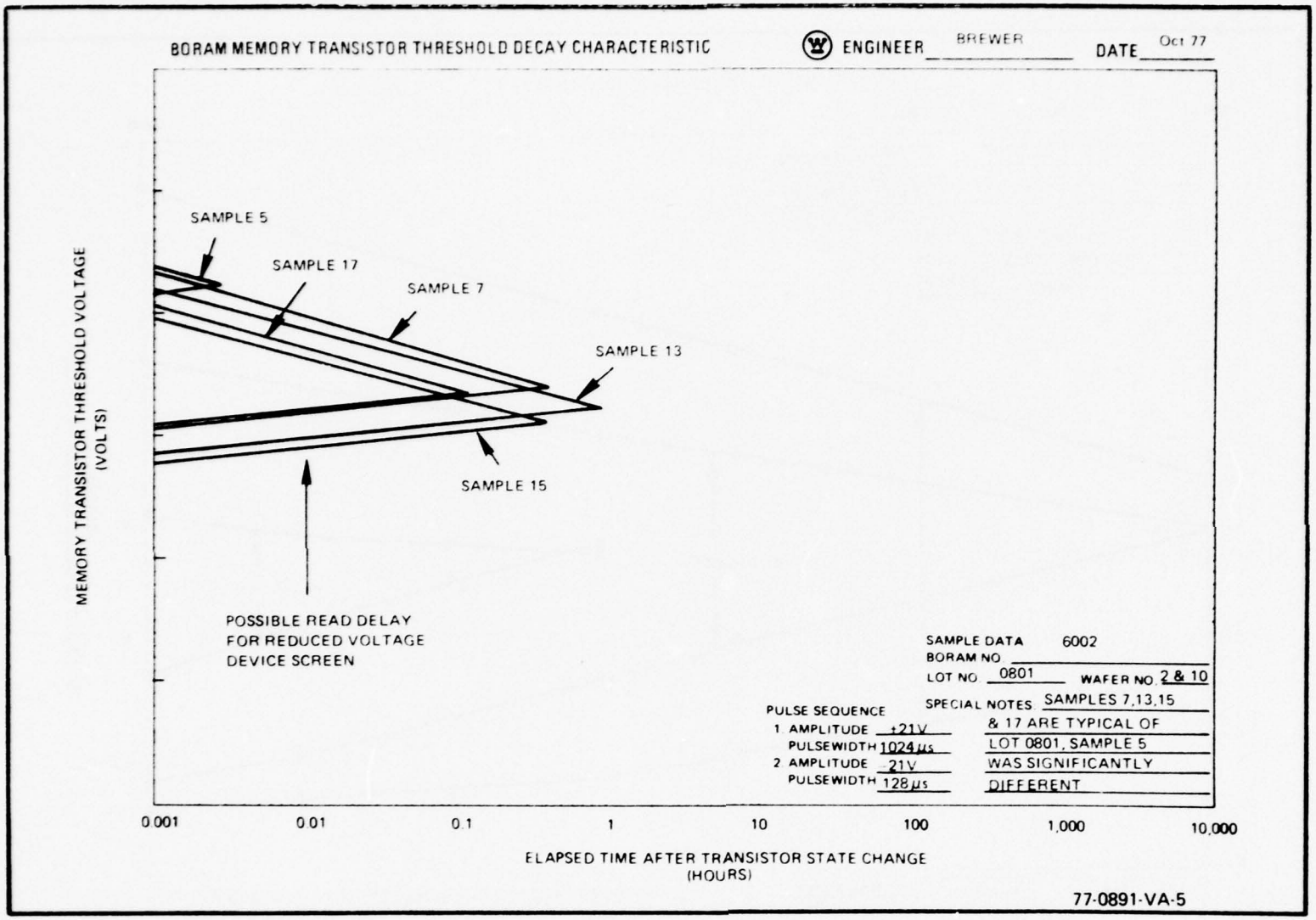

Figure 1-10. Threshold Voltage Windows for Reduced Voltage Screen

in a saturated high conduction state. If the erase voltage amplitude were reduced this initial condition would be changed. The write pulse response would in effect be tested in the non-saturated mode - a condition which should never exist.

Paragraph 1. 1. 2. 4 presented a description of exactly how the retention screen was mechanized for the characterization project. Erase and read operations were performed at nominal supply voltages. The VGG supply voltage was progressively reduced in 0. 5 volt decrements for writing until a data read out failure occurred.

Table 1-15 shows the results obtained from the characterization test on BORAM 6002 devices. Figure 1-11, 1-12 and 1-13 show the distributions of pass voltages at each temperature. Apparently the circuit enjoys the greatest operating margin at high temperature. In practice this screening technique would be used only at room temperature.

On the basis of this limited amount of distribution data a retention screen

TABLE 1-15
RETENTION SCREEN STATISTICS

Sample Size	Ambient Temperature (degrees C)	Mean Pass Voltage (Volts)	Standard Deviation (Volts)	Highest Voltage (Volts)	Lowest Voltage (Volts)
43	+125	25.174	0.487	27.0	24.00
44	+25	25.648	0.695	28.0	25.00
29	−55	26.172	0.879	28.0	24.00

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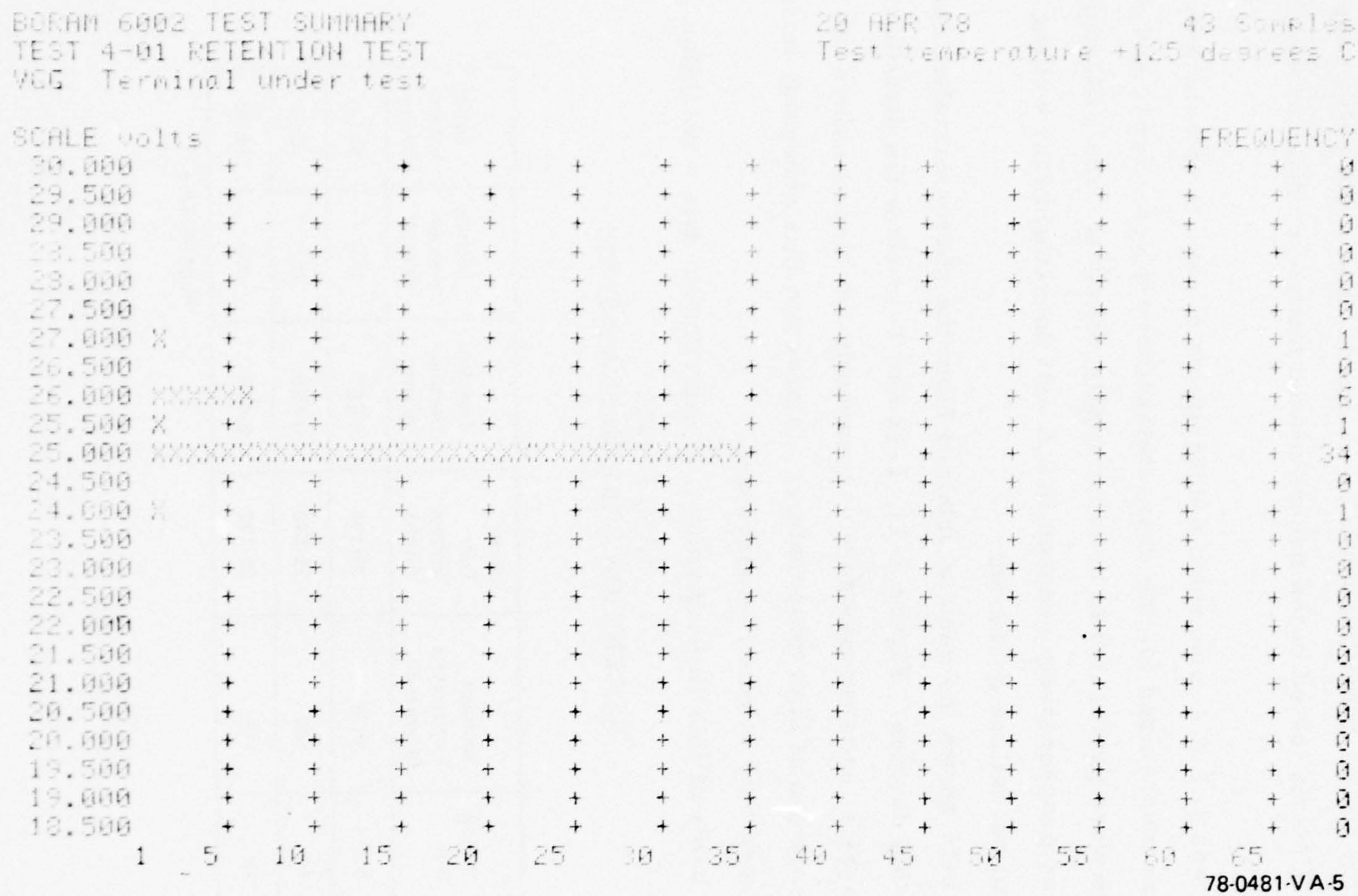

Figure 1-11. Retention Test 125° C Histogram

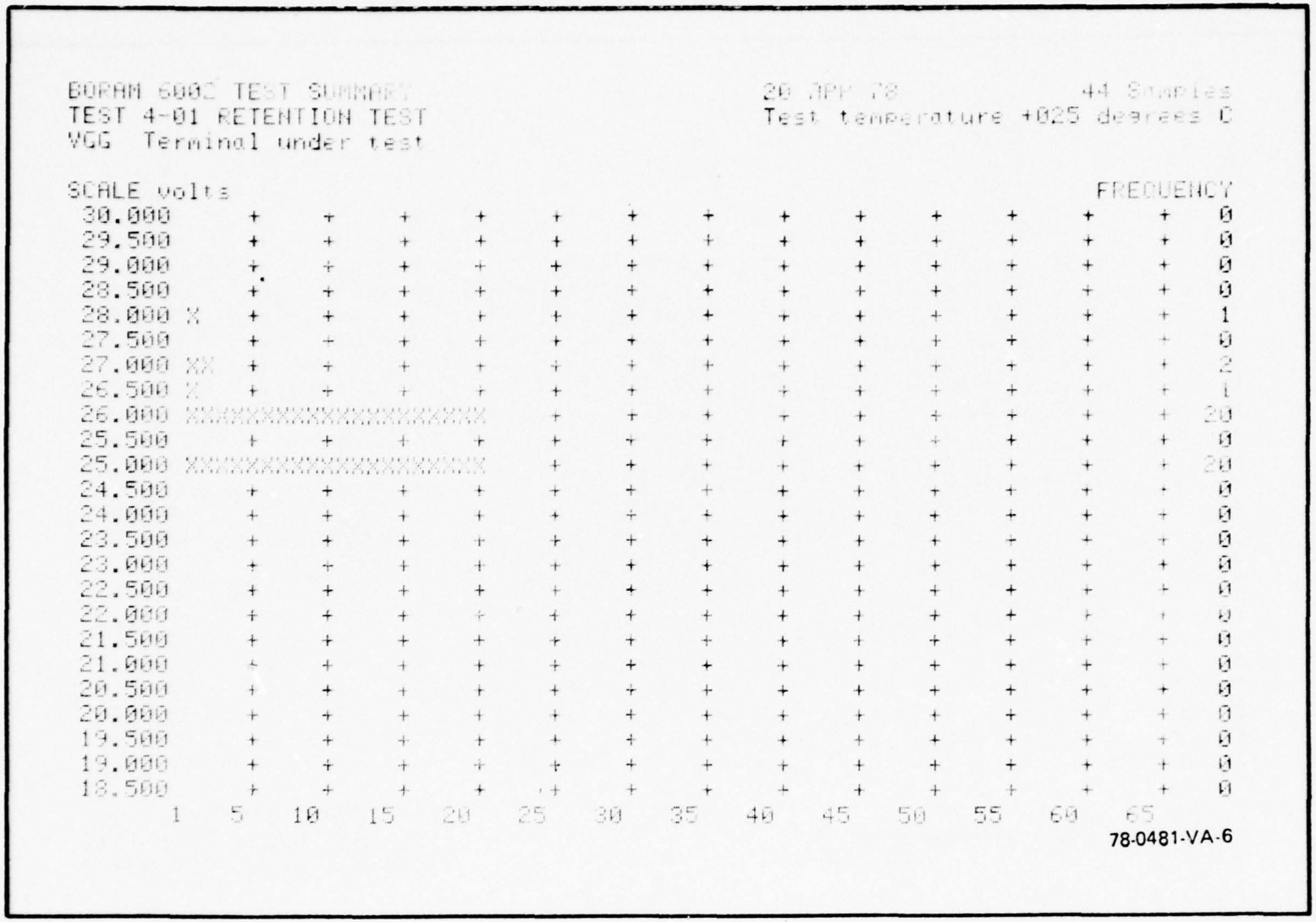

Figure 1-12. Retention Test 25°C Histogram

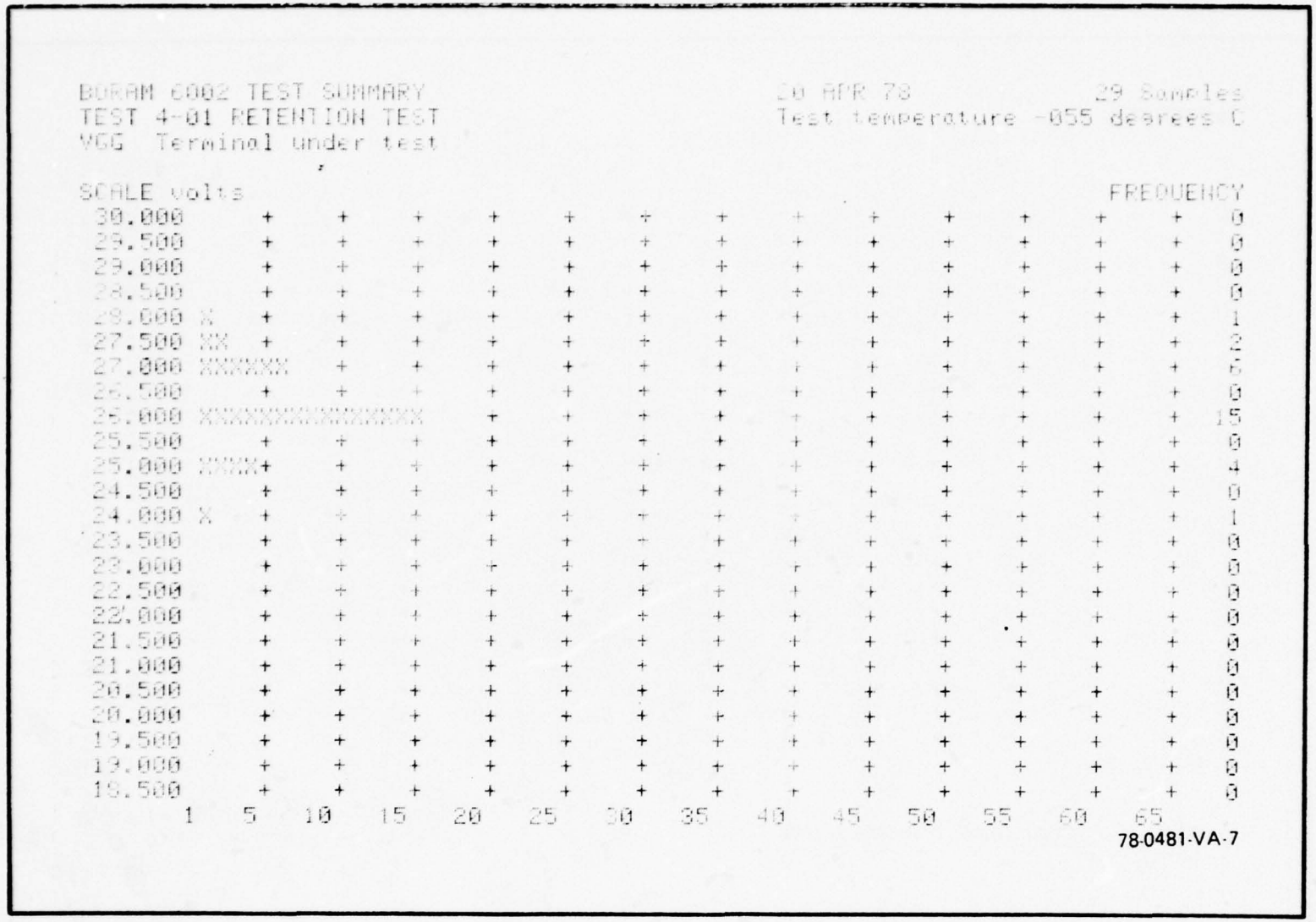

Figure 1-13. Retention Test -55°C Histogram

test limit of 27 volts has been established for wafer probe test. In this case the parts will be required to pass a zero pattern and a one pattern written with VGG at -27 volts.

As a follow up action it is planned to identify a number of die which fail this criteria. These parts will be packaged, tested using the characterization program, and observed for retention properties.

1.2.3 Erase Recovery Tests

The purpose of "Erase Recovery" tests is to examine each cell for adequate pulse response. The operation of an MNOS BORAM memory cell is dependent on the past history of data storage. As documented in paragraph 1.1.2.6 four tests are performed which store the complement of a particular data pattern 100 times, then store the data pattern one time. The last data pattern is read back to verify chip operation.

This constitutes a worst case situation for normal device operation. One transistor in the cell is erased 101 times, and then is written. The "erase recovery" name describes this case. The other transistor is erased and written alternately 100 times, and then is erased once.

The transistor which was erased 101 times can be expected to be in hard saturation. After writing this device with a single pulse the least negative threshold voltage level associated with normal cell operation can be expected. The second transistor is pulsed from the written state to the cleared state. This is also the most marginal erase condition.

Empirical results tend to support the need for an erase recovery test. Devices with marginal pulse response are detected. These same devices can pass a simple erase write of several patterns. Use of single erase write tests with marginal pulse response devices shows nonrepeatable results.

In planning the erase recovery test sequence the question of assuring margins had to be considered. One aspect of this matter is the choice of the number of times the pattern should be stored before reversal. On small samples of parts no difference was noted between 100 and 10 repetitions.

The smaller number was finally selected to save test time at wafer test.

Other alternatives for insuring operating margins will be explored in the future. For example, it may be desirable to use a reduced VGG voltage or narrow pulse widths when the last data pattern is written.

1.2.4 Group Operations Test

The BORAM 6002 device may be erased in the chip mode or the group mode. A chip erase affects all 2048 cells in the device. A group erase operates only on 128 bits associated with four rows in the RAM.

The term "group" was derived from nomenclature used to describe the data organization within BORAM storage systems. The choice of a 128 bit clear was made after a study of the data block sizes required by different users.

A point of concern with group mode operation was to be sure that clearing one group did not disturb the contents of unaddressed groups. The group operations test was designed to efficiently verify the absence of gross disturb effects while confirming proper memory operation.

The scheme employed was to begin at the high order address and go through the entire chip erasing and writing groups. Then the entire chip is read. The procedure is then repeated with the complementary data pattern beginning at the low order address. In this manner each is exposed to whatever transients are associated with adjacent group erase.

1.2.5 Read Disturb Tests

To read the contents of a storage cells it is necessary to operate the two transistors in some manner that will compare the threshold voltages and yield a logical one or zero output. If the reading process causes a threshold shift, a disturb effect is said to exist. The magnitude and nature of disturb effects are a function of the design of the read circuitry.

In the BORAM 6002 chip the memory transistors are operated as source followers for reading. Disturb effects are believed to be minimal. By design, any disturb action should enhance the written state. If a device is read

continuously the net disturb action should increase the threshold voltage window, and should extend the nonvolatile data retention time.

A read disturb test was included in the characterization program with some mixed feelings about its utility. Army specification SCS503 requires that each chip be demonstrated as being capable of 10 reads without loss of data. The characterization program performs 1000 read operations. In samples tested to date, no part which has passed the functional test requirements has failed the read disturb test.

It appears that a more meaningful investigation of possible read disturb action should cycle parts out to 10^{11} or 10^{12} reads. The relationship between retention and reading should be treated, and possible changes in characteristics with endurance cycling should be examined. These experiments were beyond the scope of the present study.

1.3 STATIC PARAMETER TESTS AND RESULTS

Table 1-7 in text above listed 20 static parameter tests which were included in the characterization program. This discussion will review the rationale for each group of tests, and will present test results.

1.3.1 Data Summary

Tables 1-16, 1-17 and 1-18 provide a statistical summary of test results obtained from the characterization program at 125°C, 25°C and -55°C. The data is identified by test number. The static parameter tests are numbered 3-01 to 3-20. These tables were prepared by the data reduction program discussed in paragraph 1.1.3.

1.3.2 Leakage Current Observations

The conceptually simple measurement of leakage current involves some problems which require practical compromises. These measurements are performed to detect gross insulator or reverse biased junction defects. A voltage difference between the terminal under test and all other device terminals is forced, and the resulting current flow is measured.

A typical input node may exhibit a few picoamperes of current. A few

TABLE 1-16
STATIC PARAMETER 125°C TEST RESULTS

DSPAM 6002 TEST SUMMARY 30 APR 78 43 Samples
Test Temperature +125 degrees C

TEST NUMBER	UNITS	MEAN	STD DEV sigma	HI LIMIT +3 sigma	LO LIMIT -3 sigma	HIGH	LOW
3-01	microamps	0.969	2.469	8.375	0.000	10.240	0.005
3-02	microamps	0.044	0.024	0.116	0.000	0.105	0.005
3-03	microamps	0.044	0.027	0.124	0.000	0.125	0.005
3-04	microamps	0.047	0.028	0.133	0.000	0.125	0.005
3-05	microamps	0.060	0.031	0.153	0.000	0.140	0.010
3-06	microamps	0.284	1.554	4.946	0.000	10.235	0.005
3-07	microamps	0.313	1.554	4.975	0.000	10.235	0.005
3-08	microamps	0.046	0.025	0.121	0.000	0.115	0.005
3-09	microamps	0.039	0.023	0.107	0.000	0.095	0.005
3-10	microamps	0.040	0.026	0.117	0.000	0.105	0.005
3-11	microamps	0.050	0.036	0.160	0.000	0.150	0.005
3-12	microamps	0.038	0.022	0.104	0.000	0.110	0.005
3-13	volts	12.652	0.280	13.493	11.812	13.250	12.100
3-14	volts	1.613	0.158	2.087	1.138	1.950	1.300
3-15	microamps	1.237	7.232	22.934	0.000	47.550	0.050
3-16	milliamps	9.120	0.854	11.683	6.557	11.150	7.800
3-17	milliamps	19.964	2.509	27.491	12.437	24.800	15.900
3-18	milliamps	18.414	1.682	23.461	13.367	22.450	15.750
3-19	milliamps	9.041	0.834	11.542	6.539	11.050	7.750
3-20	milliamps	11.053	1.079	14.274	7.833	13.700	9.400
4-01	volts	25.174	0.487	26.634	23.715	27.000	24.000
5-01	volts	2.330	0.064	2.522	2.139	2.515	2.205
5-02	volts	2.969	1.890	8.638	0.000	11.050	2.300
5-03	volts	12.109	2.135	18.513	5.705	13.350	2.300
5-04	volts	2.174	0.114	2.515	1.834	2.550	1.900
5-05	volts	26.028	0.176	26.557	25.499	26.400	25.550

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TABLE 1-17
STATIC PARAMETER 25°C TEST RESULTS

FURAM 6002 TEST SUMMARY 20 APR 78 44 Samples
Test Temperature +025 degrees C

TEST NUMBER	UNITS	MEAN	STD DEV sigma	HI LIMIT +3 sigma	LO LIMIT -3 sigma	HIGH	LOW
3-01	microamps	0.809	2.459	8.188	0.000	10.240	0.010
3-02	microamps	0.041	0.013	0.081	0.001	0.085	0.020
3-03	microamps	0.022	0.009	0.047	0.000	0.045	0.005
3-04	microamps	0.028	0.008	0.052	0.004	0.045	0.005
3-05	microamps	0.028	0.012	0.064	0.000	0.085	0.015
3-06	microamps	0.255	1.540	4.874	0.000	10.235	0.010
3-07	microamps	0.267	1.539	4.884	0.000	10.236	0.010
3-08	microamps	0.029	0.009	0.057	0.001	0.045	0.015
3-09	microamps	0.026	0.007	0.048	0.005	0.040	0.010
3-10	microamps	0.036	0.049	0.184	0.000	0.350	0.015
3-11	microamps	0.025	0.006	0.043	0.007	0.040	0.015
3-12	microamps	0.011	0.004	0.022	0.000	0.020	0.005
3-13	volts	12.989	0.238	13.702	12.275	13.500	12.550
3-14	volts	1.384	0.131	1.777	0.991	1.650	1.150
3-15	microamps	1.522	9.623	30.391	0.000	63.900	0.050
3-16	milliamps	11.025	0.952	13.882	8.168	13.150	9.350
3-17	milliamps	24.063	3.274	33.886	14.239	29.300	18.800
3-18	milliamps	21.989	2.512	29.526	14.451	26.100	18.850
3-19	milliamps	10.902	0.941	13.724	8.080	13.000	9.250
3-20	milliamps	13.234	1.202	16.841	9.627	15.800	11.200
4-01	volts	25.648	0.695	27.734	23.562	28.000	25.000
5-01	volts	2.394	0.063	2.582	2.206	2.580	2.285
5-02	volts	2.932	1.623	7.802	0.000	9.800	2.350
5-03	volts	12.394	2.173	18.913	5.876	13.500	2.350
5-04	volts	3.459	0.453	4.819	2.099	4.100	2.250
5-05	volts	26.059	0.252	26.814	25.304	27.000	25.600

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TABLE 1-18
STATIC PARAMETER -55°C TEST RESULTS

SORAM 6002 TEST SUMMARY 20 APR 78 24 Samples
Test temperature -055 degrees C

TEST NUMBER	UNITS	MEAN	STD DEV sigma	HI LIMIT +3 sigma	LO LIMIT -3 sigma	HIGH	LOW
3-01	microAMPS	7.213	3.057	16.384	0.000	10.240	0.100
3-02	microAMPS	6.171	3.397	16.363	0.000	10.235	0.130
3-03	microAMPS	6.937	3.650	17.886	0.000	10.235	0.060
3-04	microAMPS	3.977	3.385	14.131	0.000	10.235	0.045
3-05	microAMPS	5.908	3.525	16.482	0.000	10.235	0.030
3-06	microAMPS	8.227	3.313	18.167	0.000	10.235	0.325
3-07	microAMPS	8.646	2.615	16.491	0.801	10.235	1.975
3-08	microAMPS	7.472	3.574	18.196	0.000	10.235	0.130
3-09	microAMPS	7.385	3.324	17.359	0.000	10.235	1.510
3-10	microAMPS	4.556	3.543	15.185	0.000	10.235	0.065
3-11	microAMPS	8.007	3.378	18.142	0.000	10.235	0.365
3-12	microAMPS	5.398	3.182	14.944	0.000	10.235	0.035
3-13	volts	13.443	0.202	14.048	12.838	13.800	12.950
3-14	volts	1.084	0.124	1.456	0.712	1.450	0.900
3-15	microAMPS	17.030	31.039	110.153	0.000	102.440	0.300
3-16	milliAMPS	14.522	0.892	17.197	11.848	17.250	12.450
3-17	milliAMPS	31.884	4.703	45.895	17.774	39.700	28.050
3-18	milliAMPS	29.053	1.905	34.767	23.340	34.050	24.750
3-19	milliAMPS	14.176	0.865	16.772	11.580	17.100	12.350
3-20	milliAMPS	16.910	1.065	20.104	13.717	20.550	14.700
4-01	volts	26.172	0.879	28.810	23.535	28.000	24.000
5-01	volts	2.307	0.472	3.724	0.889	2.605	0.830
5-02	volts	2.669	1.959	8.747	0.000	8.750	0.600
5-03	volts	11.433	3.922	23.199	0.000	13.300	0.950
5-04	volts	4.014	0.442	5.338	2.689	4.450	3.600
5-05	volts	25.271	0.970	28.181	22.361	25.900	21.350

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nodes may have microampere level currents. The wide variation of current values and the need to set a measurement scale for automatic test equipment is in conflict. For the characterization program, measurements were performed using a 10 microampere full scale setting. For this condition the equipment accuracy is ±0.05 microamperes.

This choice of scales allows visibility of only the few current values in the microampere range. All low current readings simply result in random indications on the order of 0.05 microamperes.

During the characterization project measurements were attempted at -55°C, 25°C and 125°C. The leakage currents observed at -55°C were inaccurate because of surface leakage on the test fixtures. A considerable amount of frosting was present during the experiment. Since other data taken at that temperature was valid, and leakage currents are normally well behaved at low temperature, the test was not repeated.

1.3.2.1 Chip Select Leakage

Figures 1-14 and 1-15 show the chip leakage distributions at 125°C and 25°C. At room temperature six parts were observed to have leakage in excess of 0.5 microamperes. Two parts showed full scale readings of 10.240 microamperes.

It appears that the use of 40 volts for this test on the BORAM 6002 is extreme. The tail edge of the normal breakdown characteristic goes below 40 volts. A better choice appears to be 37.5 volts. The high leakage currents observed in the sample where due to junction breakdown, not to defective insulators or junctions. Testing at 37.5 volts allows for more than 5 percent variation in the nominal 35 volt level.

1.3.2.2 CMOS Level Input Leakages

In table 1-3 in the text above it was shown that input signals $\overline{TR}$, A0, A3/4, A1, A2, $\phi 2$, DW, A2/5, $\overline{AE}$, $\overline{MW}$, and $\phi 1$ require signal swings similar to that of CMOS devices operated at 15 volts. Each of these inputs was tested for leakage current at -20 volts. The resulting distributions for all measured inputs combined is presented in figures 1-16 and 1-17.

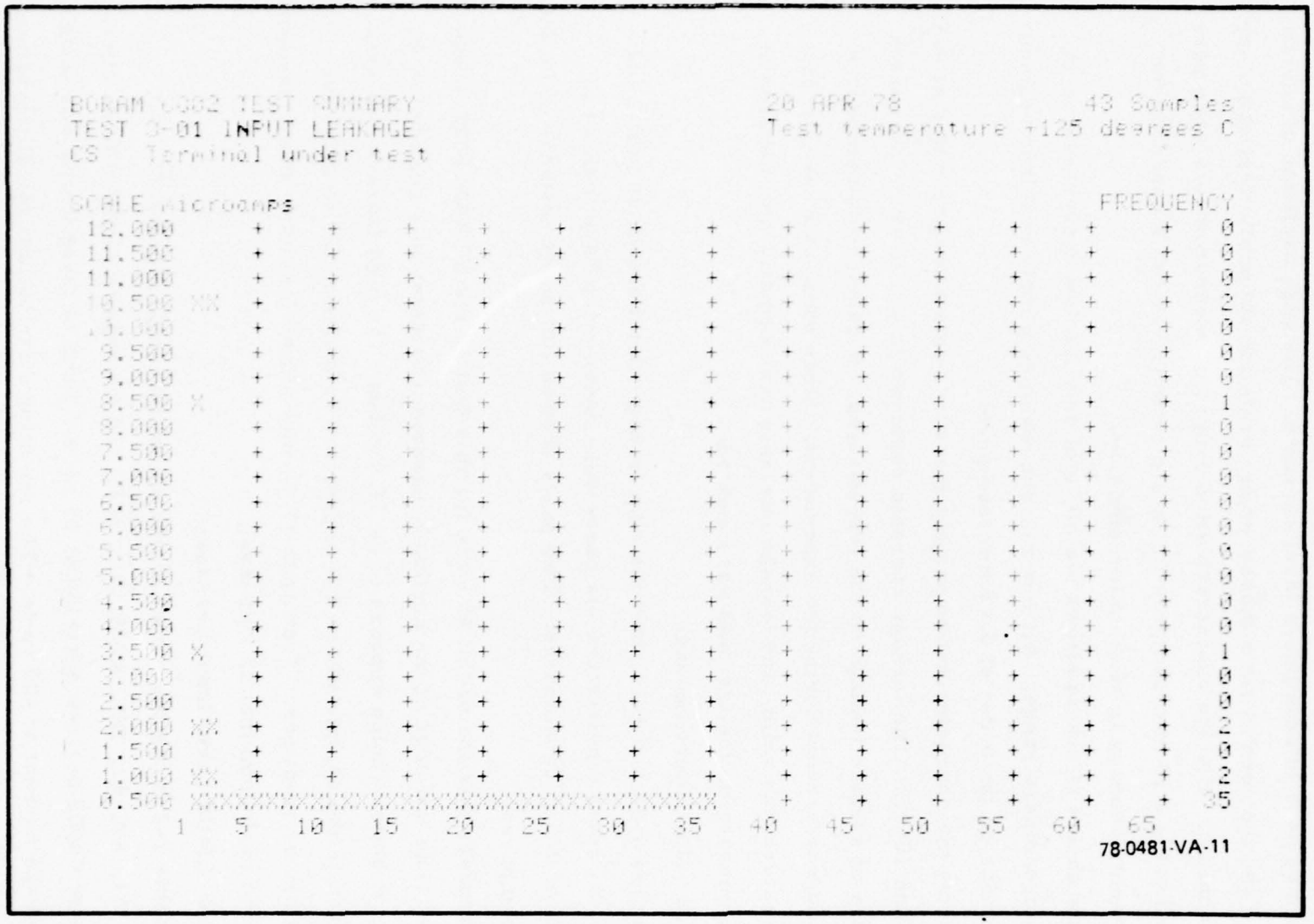

Figure 1-14. Chip Select Leakage Current at 125° C

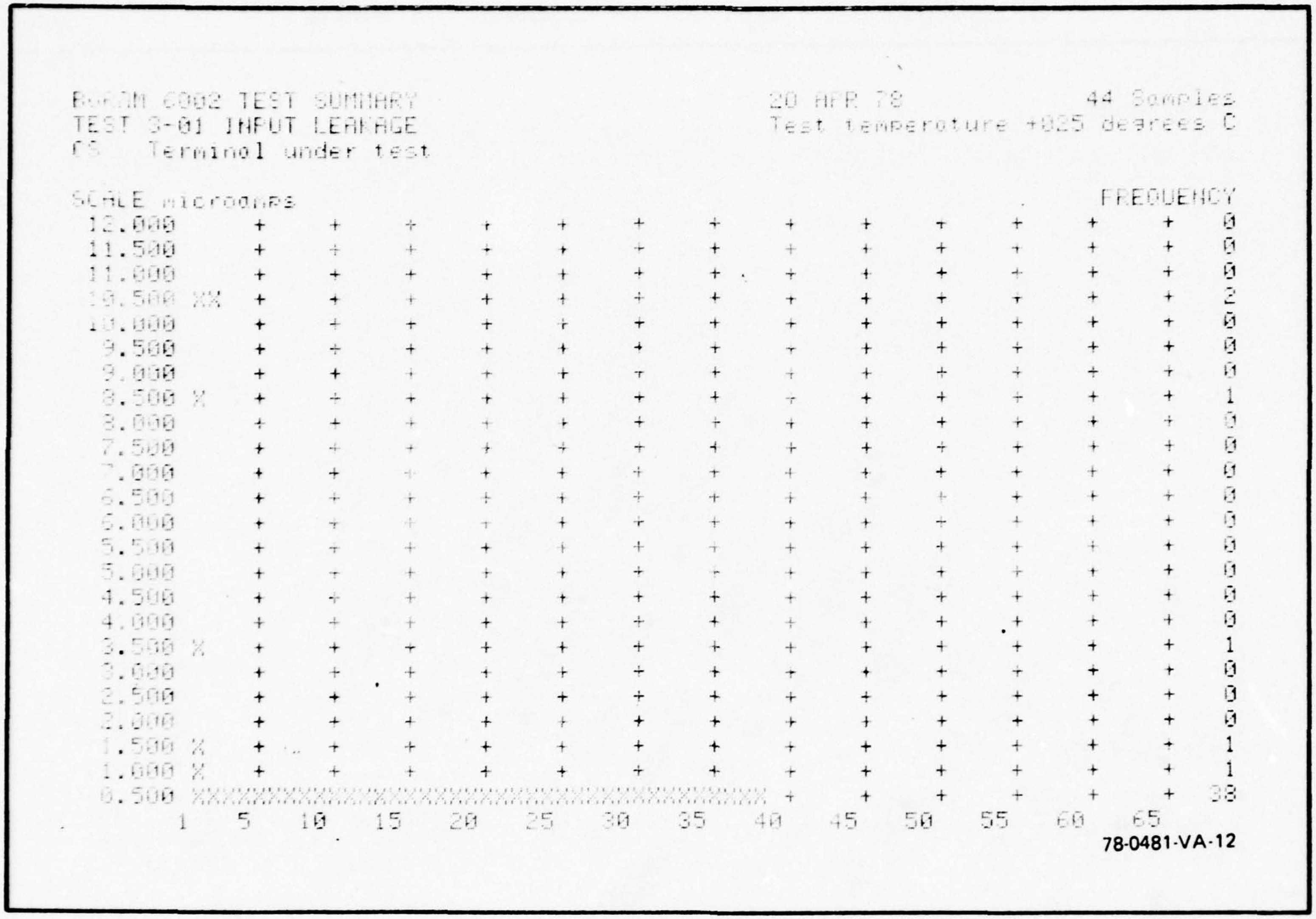

Figure 1-15. Chip Select Leakage Current at 25°C

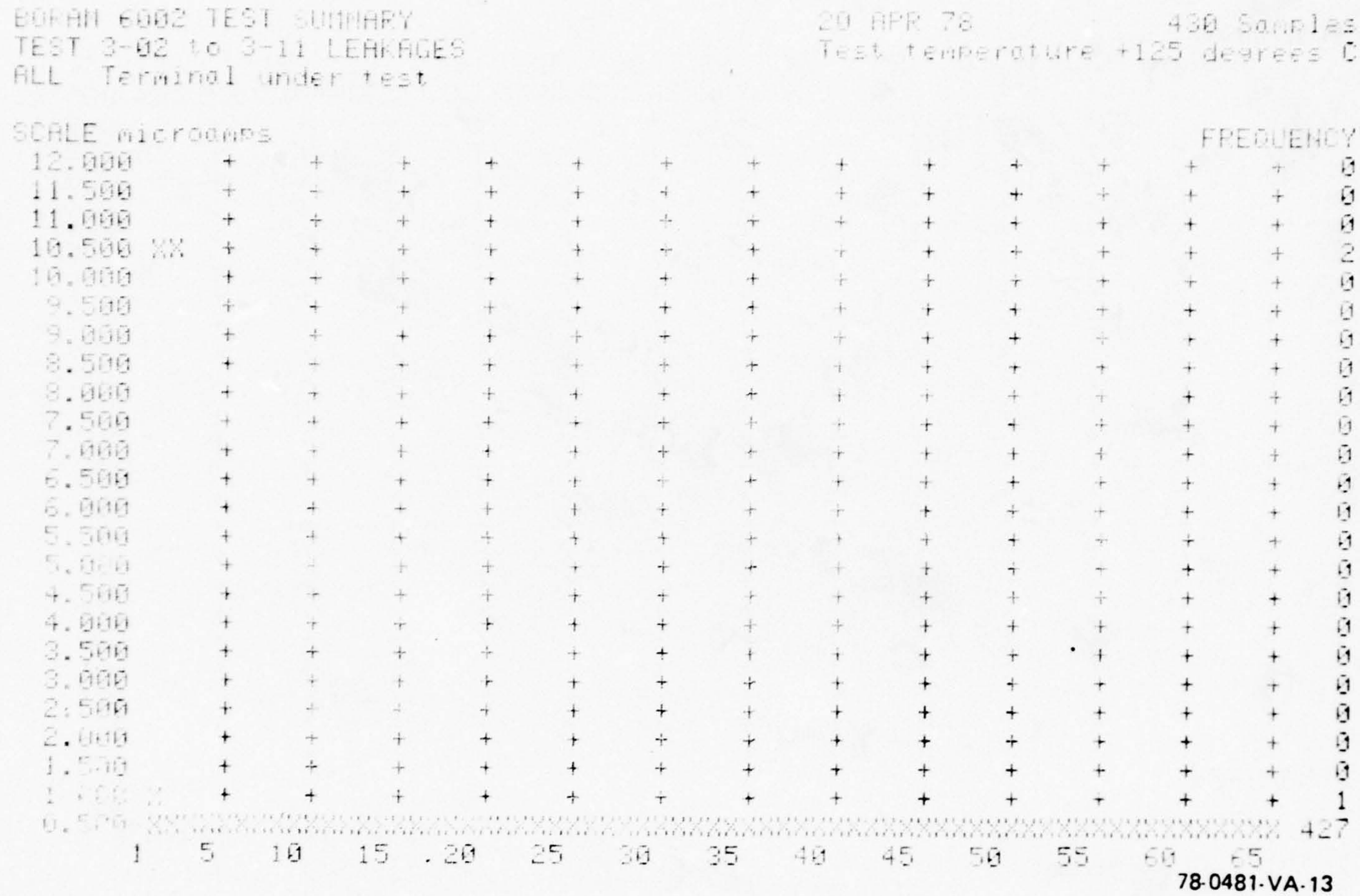

Figure 1-16. CMOS Level Input Leakages at 125°C

```
BORAM 6002 TEST SUMMARY                          20 APR 78           440 Samples
TEST 3-02 to 3-11 LEAKAGES                       Test temperature +025 degrees C
ALL  Terminal under test

SCALE microamps                                                        FREQUENCY
 12.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
 11.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
 11.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
 10.500 XX   +    +    +    +    +    +    +    +    +    +    +    +    +    2
 10.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  9.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  9.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  8.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  8.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  7.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  7.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  6.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  6.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  5.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  5.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  4.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  4.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  3.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  3.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  2.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  2.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  1.500      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  1.000      +    +    +    +    +    +    +    +    +    +    +    +    +    0
  0.500 XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX  438
        1   5   10   15   20   25   30   35   40   45   50   55   60   65
                                                               78-0481-VA-14
```

Figure 1-17. CMOS Level Input Leakages at 25°C

1.3.2.3 Tristate Leakage

The output driver in the BORAM 6002 chip enters a high impedance state when chip select $\overline{CS}$ is high. This feature allows chips in the BORAM hybrid circuit to be OR tied to a common output bus.

The tristate leakage test stresses the PN junction associated with the output drive DR terminal at 20 volts. Normal usage stress is less than 15 volts. The resulting leakage current distributions are shown in figures 1-18 and 1-19 for 125°C and 25°C.

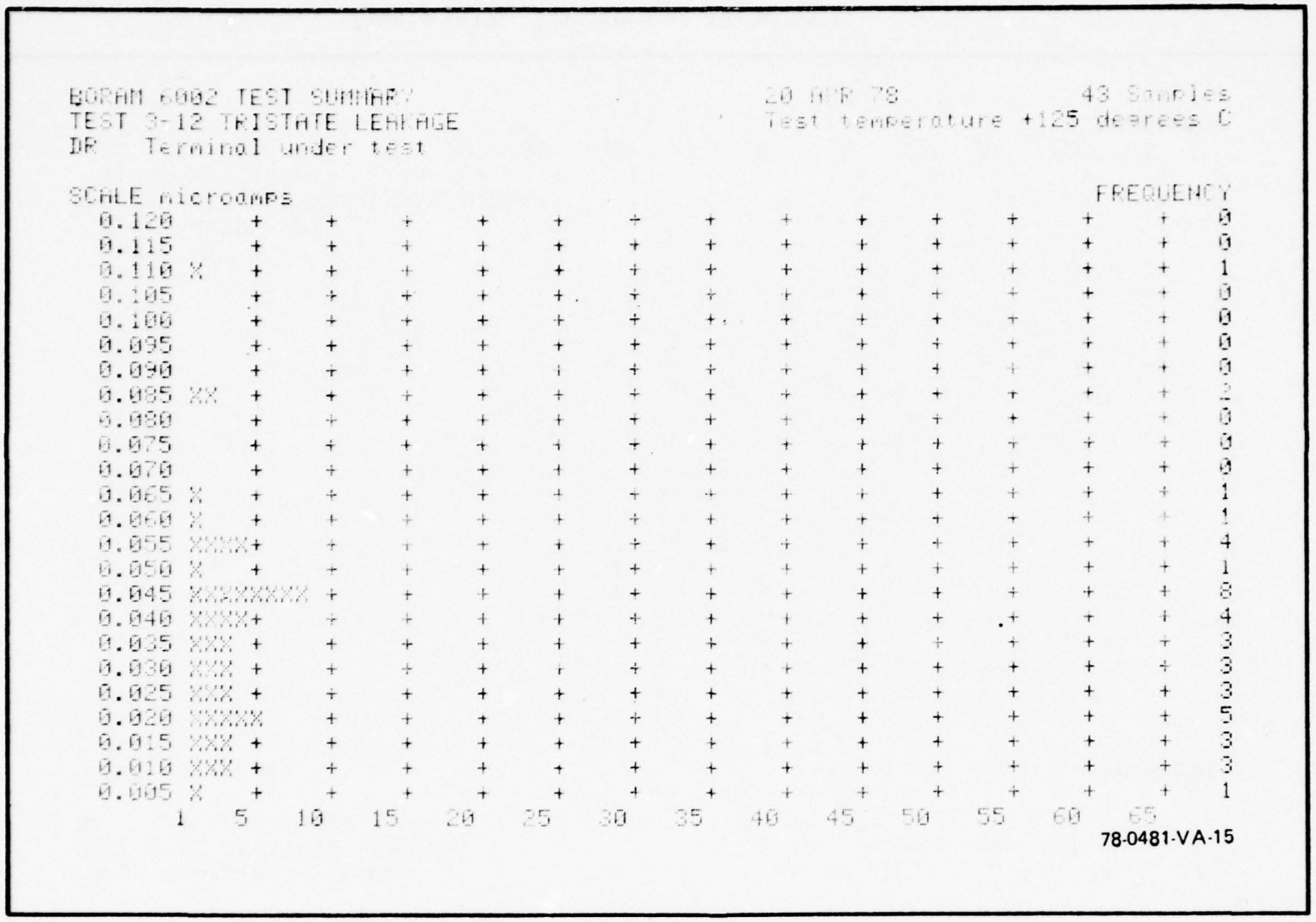

Figure 1-18. Tristate Leakage at 125°C

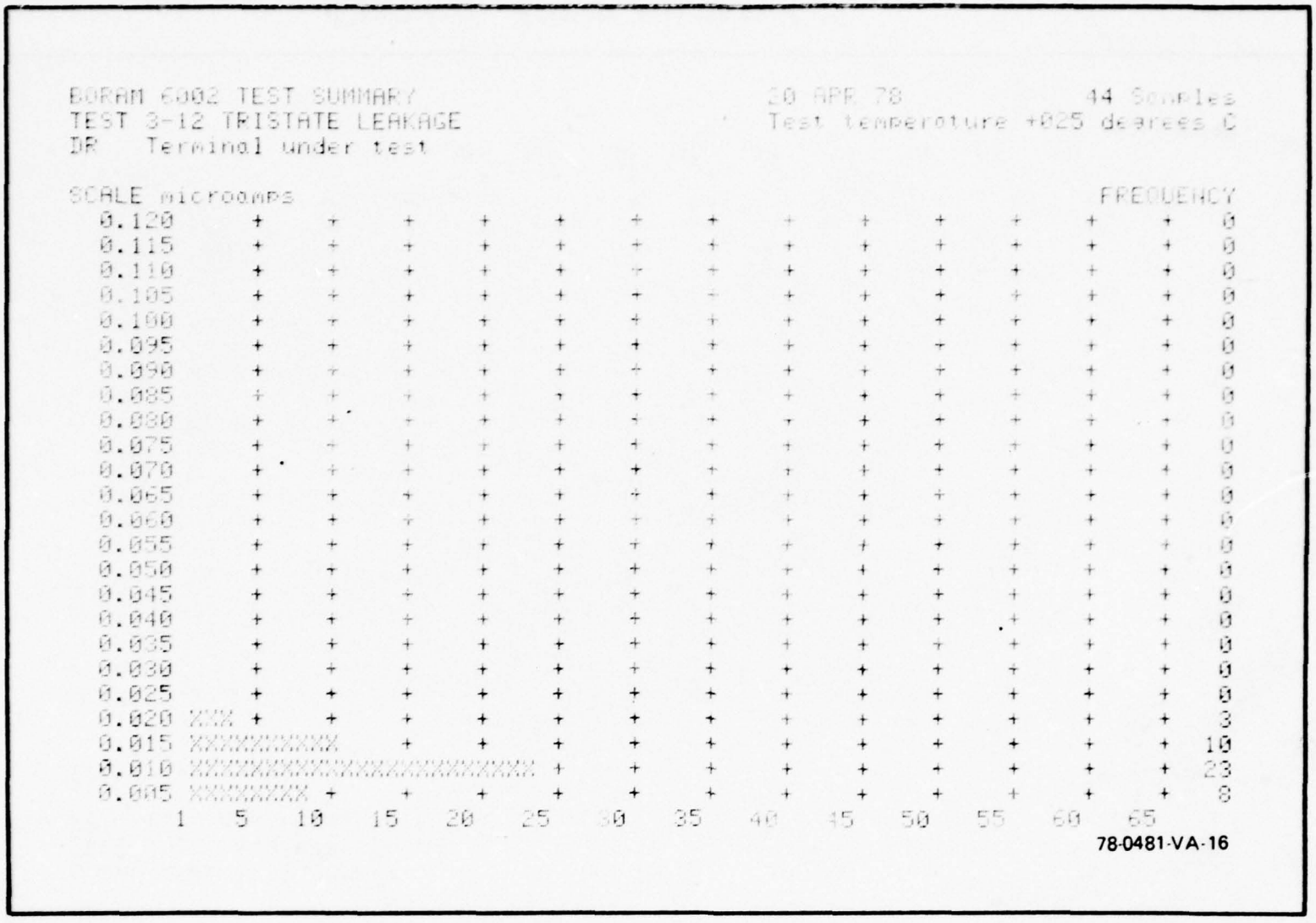

Figure 1-19. Tristate Leakage at 25°C

1.3.3 I/O Voltage Level Tests

Tests 3-13 and 3-14 of the characterization program were somewhat unusual in that several conventional device parameters are examined simultaneously. The characteristics of the on-chip two phase dynamic shift register are exploited to allow an examination of VIL, VIH, VOL and VOH. When both clock phases $\phi 1$ and $\phi 2$ are held low, the signal at the register input DW will ripple through the register and appear at the output DR.

1.3.3.1 Output Low Voltage Observations

To verify VOL (DR) and VIL (DW, $\phi 1$ and $\phi 2$) the inputs are set at a 0.25 volt guardband inside the levels given in table 1-3. DW is set at -10.25 volts. Both $\phi 1$ and $\phi 2$ are set at -14 volts. This combination constitutes the worst set of input levels to maintain the output in a low state. To check VOL the voltage from VCC to DR is measured when 5 milliamperes is forced into DR.

Figures 1-20, 1-21 and 1-22 present the results of this measurement at 125°C, 25°C and -55°C. The standard VOL voltage level for CMOS operated at a VDD of +15 volts is (15 x 0.3) + 4.5 volts. The equivalent level referred to VCC is -10.5 volts. Note that the samples were able to sink 5 milliamperes over the temperature range and remain well below -10.5 volts.

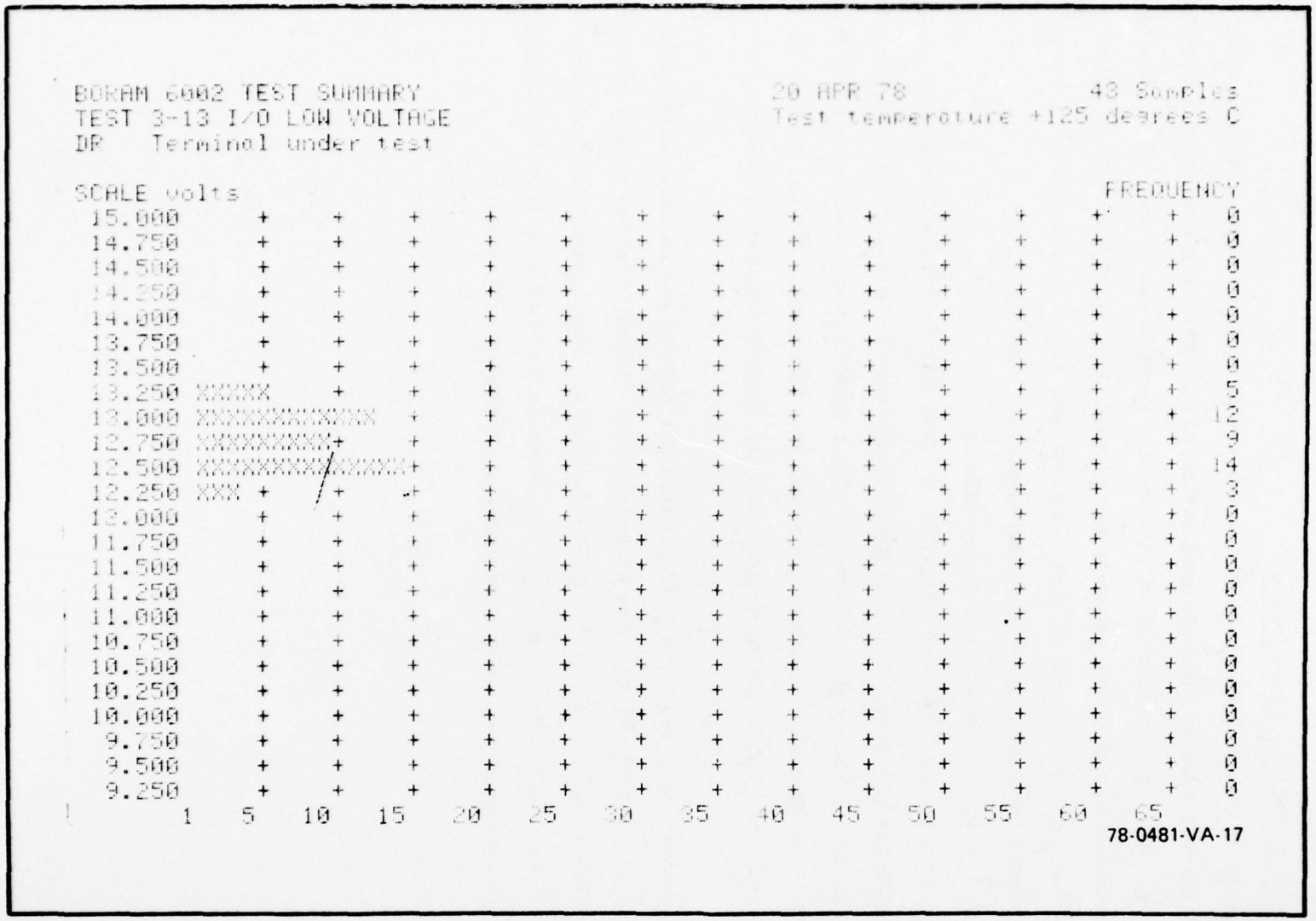

Figure 1-20. I/O Low Voltage Distribution at 125°C

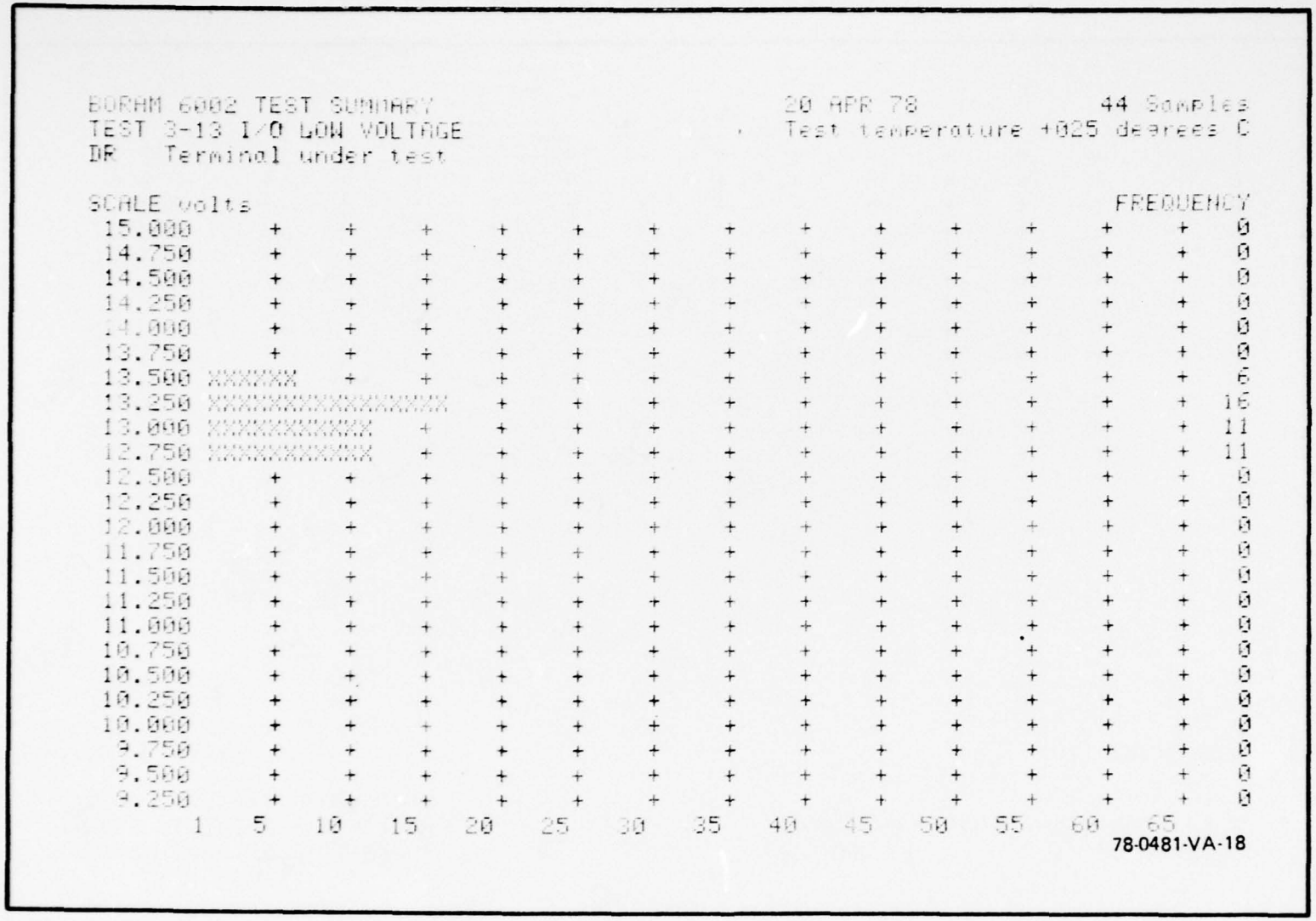

Figure 1-21. I/O Low Voltage Distribution at 25°C

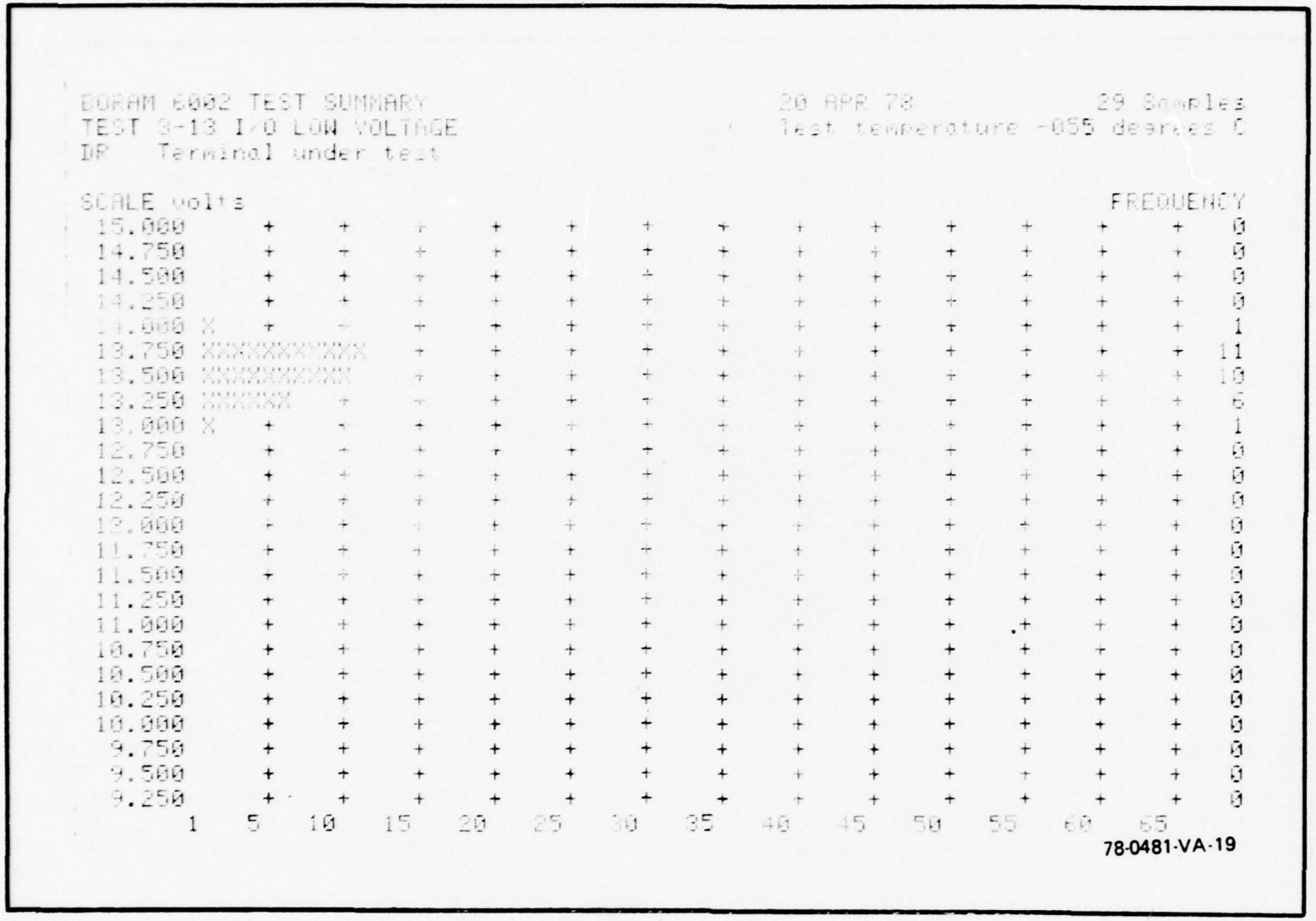

Figure 1-22. I/O Low Voltage Distribution at -55°C

1.3.3.2 Output High Voltage Observations

To verify VOH (DR), VIH (DW) and VIL (ϕ1 and ϕ2) a similar strategy is used. DW is set at -1.75 volts. Both ϕ1 and ϕ2 are set at -14 volts. To check VOH the voltage from VCC to DR is measured when 5 milliamperes is forced out of DR.

Figures 1-23, 1-24 and 1-25 shows the VOH distributions observed at 125°C, 25°C and -55°C. The standard VOH voltage level for CMOS operated at a VDD level of +15 volts is (15 x 0.7) + 10.5 volts. The equivalent level referred to VCC is -4.5 volts. All devices in population were well above this level over the temperature range while sourcing 5 milliamperes.

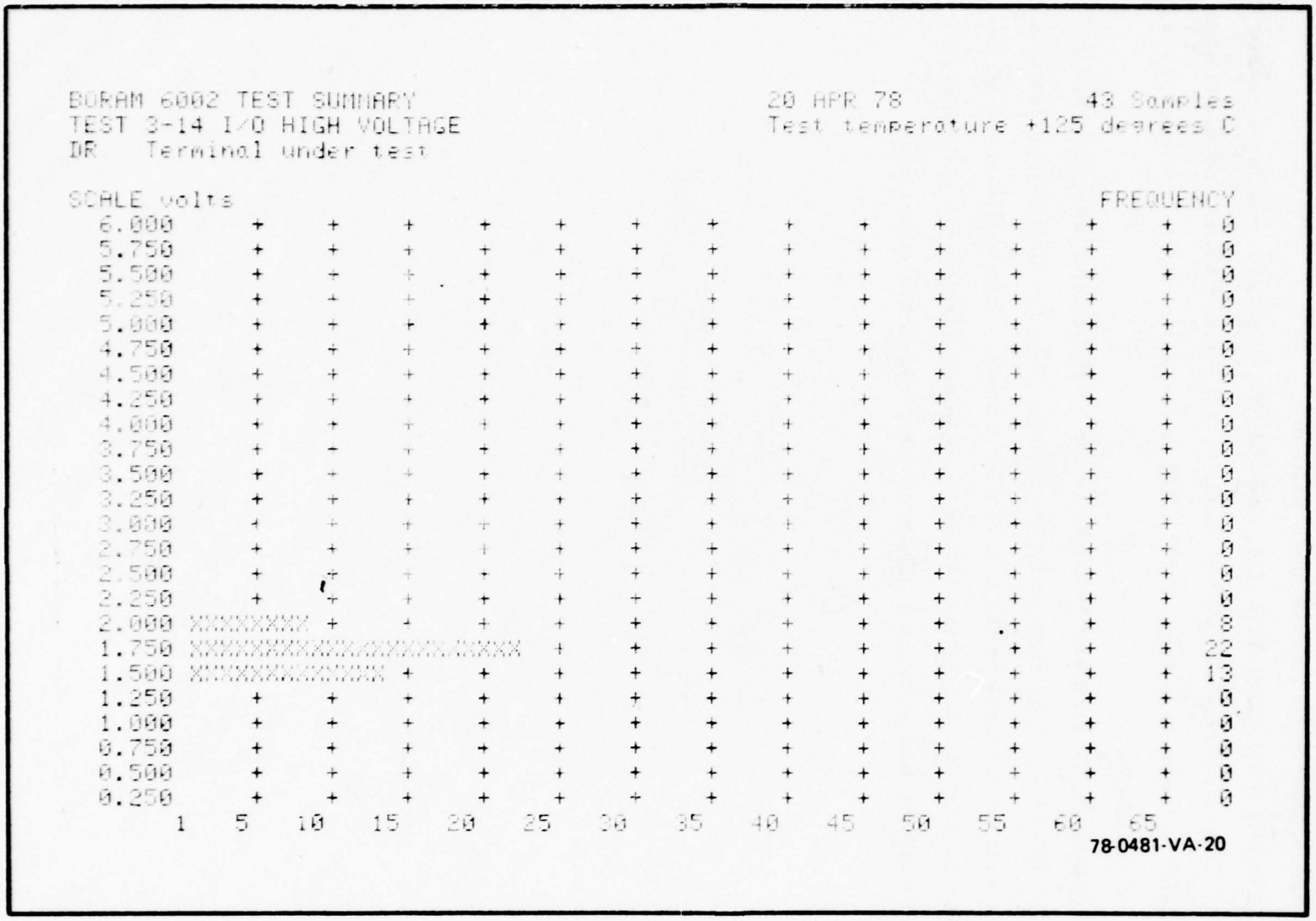

Figure 1-23. I/O High Voltage Distribution at 125°C

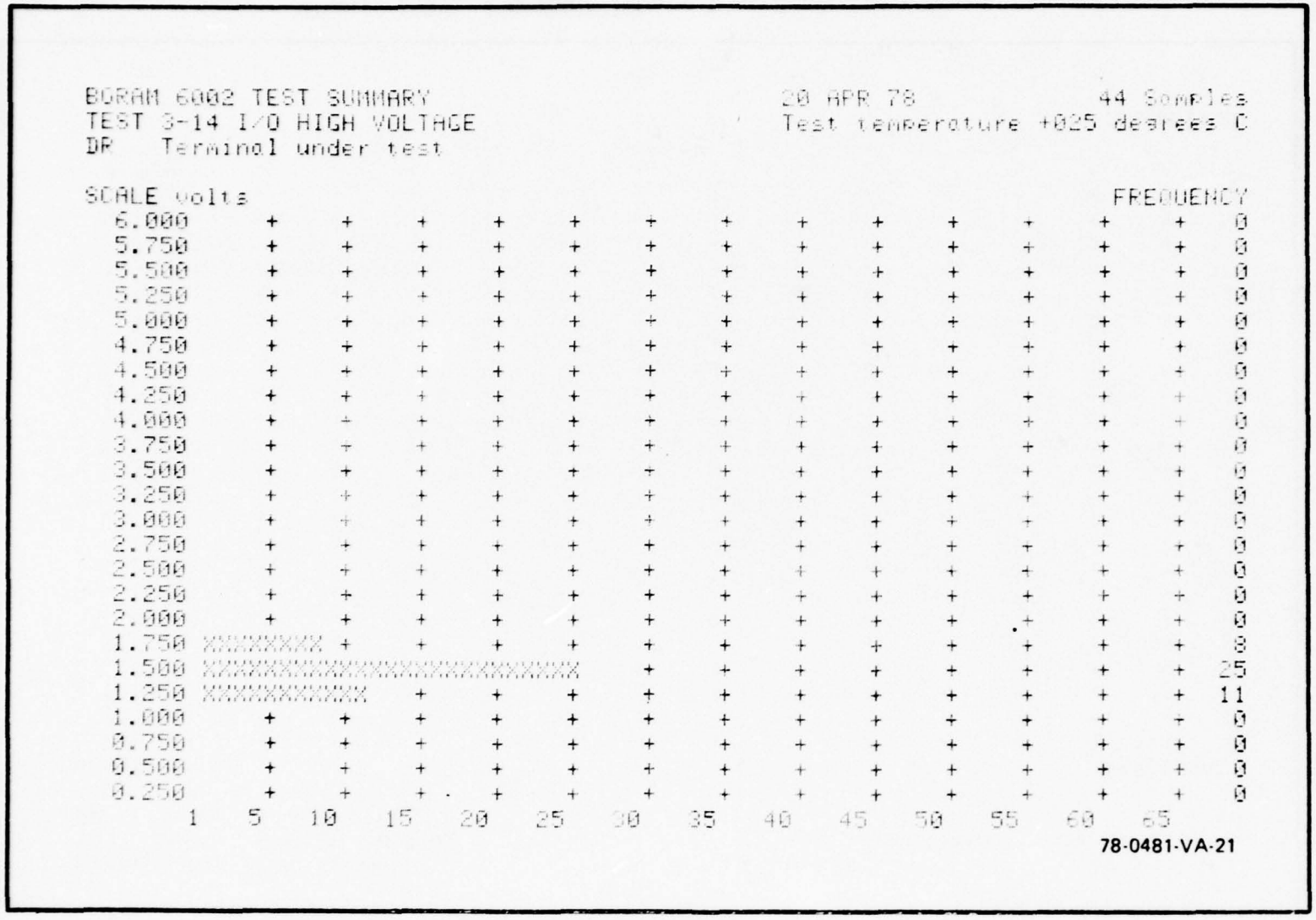

Figure 1-24. I/O High Voltage Distribution at 25°C

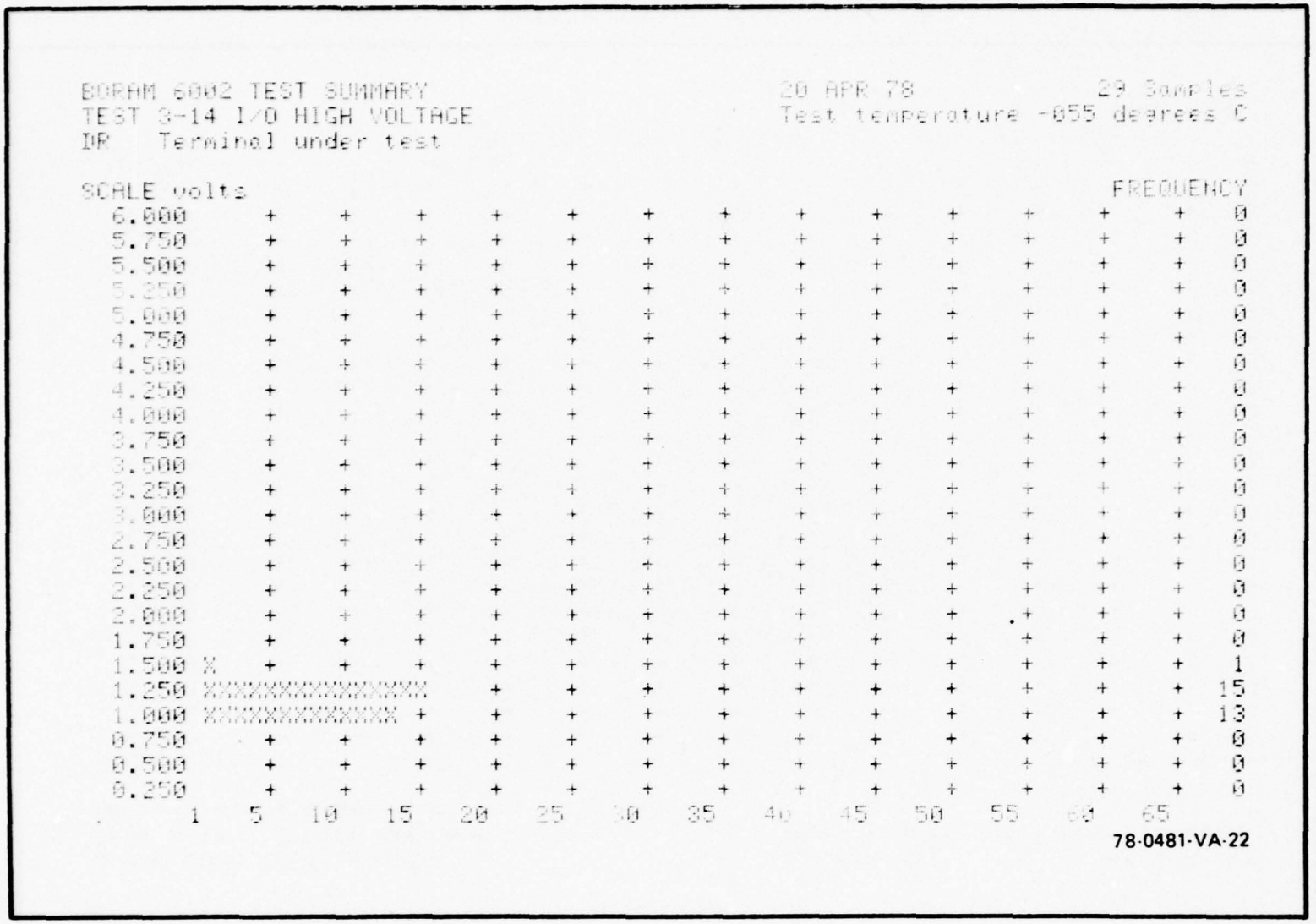

Figure 1-25. I/O High Voltage Distribution at -55°C

1.3.4 Power Dissipation and Static Mode Supply Currents

Army specification SCS503 does not place limits on static mode supply currents. It does however indicate power dissipation goals. This discussion will present measured static mode supply current data, and will explain how that data is related to power dissipation.

During the electrical test of a BORAM chip, the VCC supply current is measured in six different static modes. In this context, "static mode" means that the device terminals are held at specific DC voltages, and the DC supply current is read. In the text below each current will be referred to using the symbols:

Deselected Standby	IDS
Selected Standby	ISS
Read	IR
Write	IW
Chip Clear	ICC
Group Clear	IGC
Shift Register	ISR

The last current ISR is not one of the six static mode currents. It is the average current which flows into the shift register during the process of shifting data. For this analysis ISR is taken as 0.9mA from an analysis of the circuit operation.

1.3.4.1 Observed Supply Current Distributions

Table 1-19 summarizes the mean supply current values observed at three temperatures. Table 1-20 shows the ratio of the current at temperature extremes to the 25°C current. ISR was initially estimated at 25°C. The ISR ratios stated in table 1-20 where assumed as a means of adjusting ISR for temperature variation.

Figure 1-26 and 1-27 show the distribution of IDS at 125°C and 25°C. The observations of IDS at -55°C were believed to be invalid because of test fixture leakage currents.

Selected standby current distributions appear in figures 1-28, 1-29 and 1-30. Read current is documented in figures 1-31, 1-32 and 1-33. The

TABLE 1-19
BORAM 6002 STATIC SUPPLY CURRENT LEVELS

Static Supply Current	Symbol	VCC Terminal Current		
		−55°C mA	+25°C mA	+125°C mA
Deselected Standby	IDS	0.0017	0.0015	0.0012
Selected Standby	ISS	14.522	11.025	9.120
Read	IR	31.884	24.063	19.964
Write	IW	29.053	21.989	18.414
Chip Clear	ICC	14.176	10.902	9.041
Group Clear	IGC	16.910	13.234	11.053
Shift Register	ISR	1.19	0.9	0.75

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TABLE 1-20
STATIC SUPPLY CURRENT TEMPERATURE SENSITIVITY

Static Supply Current	Symbol	Relative VCC Terminal Current	
		I (−55)/I (25) Numeric	I (125)/I (25) Numeric
Deselected Standby	IDS	1.133	0.800
Selected Standby	ISS	1.317	0.827
Read	IR	1.325	0.830
Write	IW	1.321	0.837
Chip Clear	ICC	1.300	0.829
Group Clear	IGC	1.278	0.835
Shift Register	ISR	1.32	0.83

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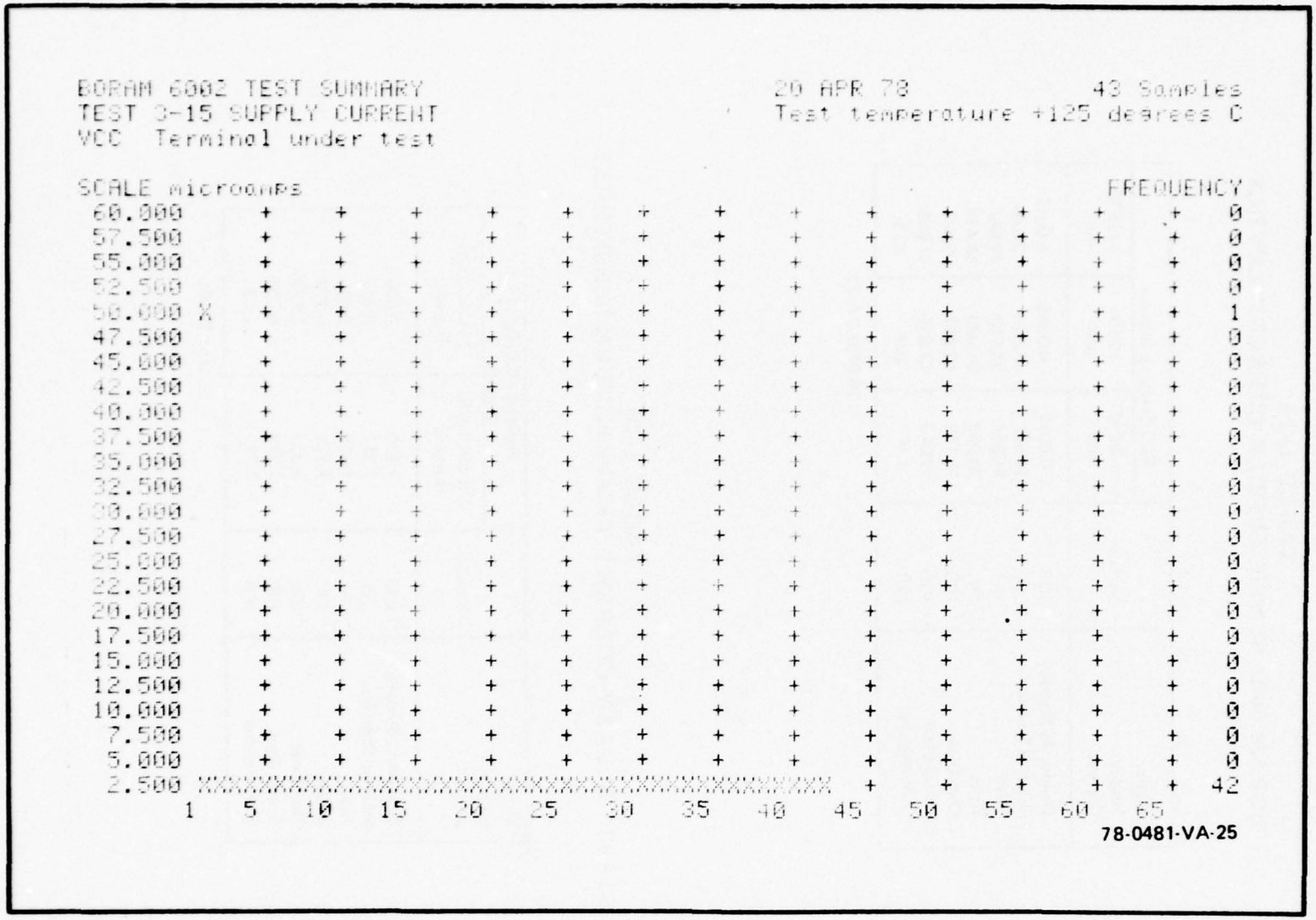

Figure 1-26. Deselected Standby Current at 125°C

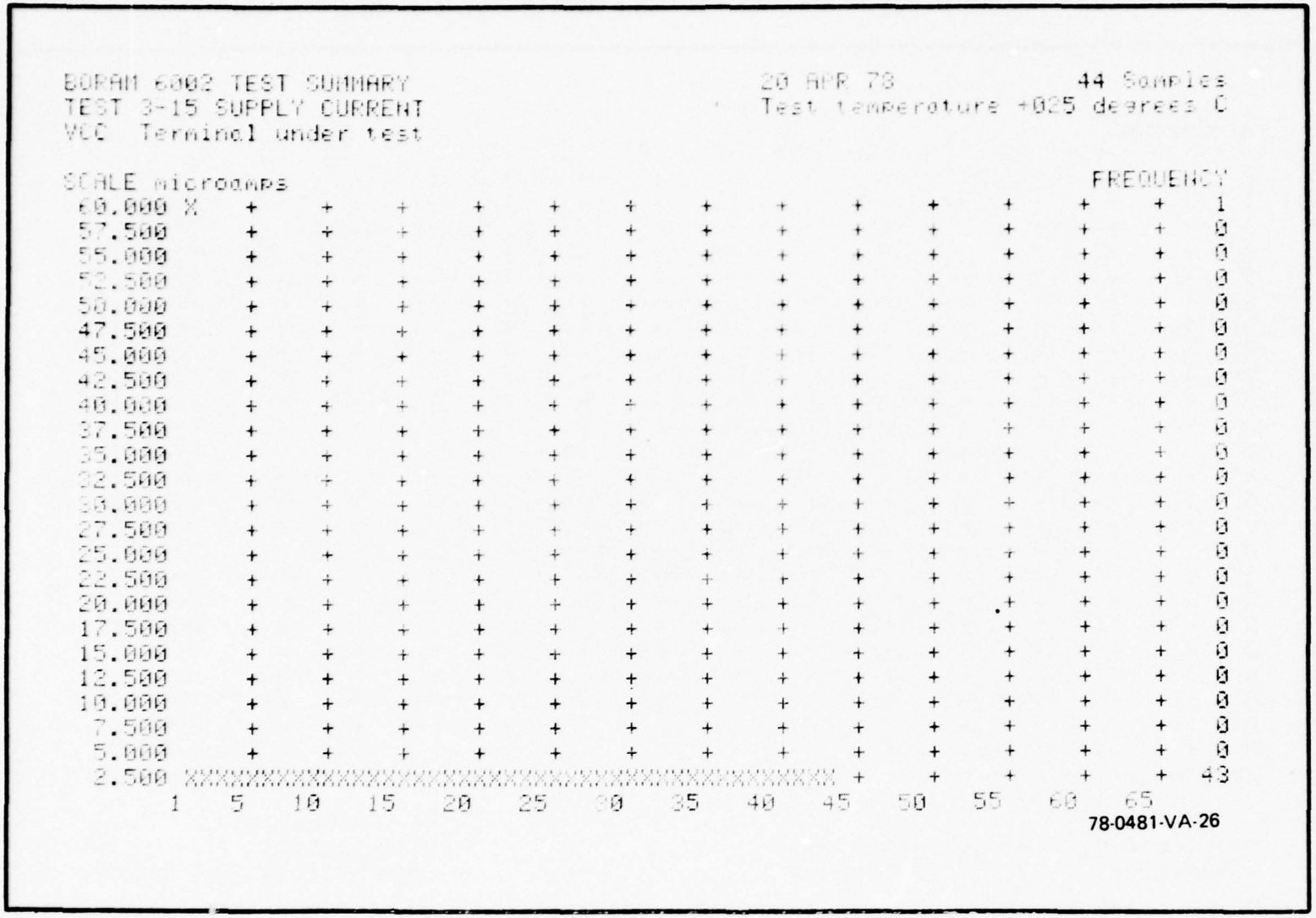

Figure 1-27. Deselected Standby Current at 25°C

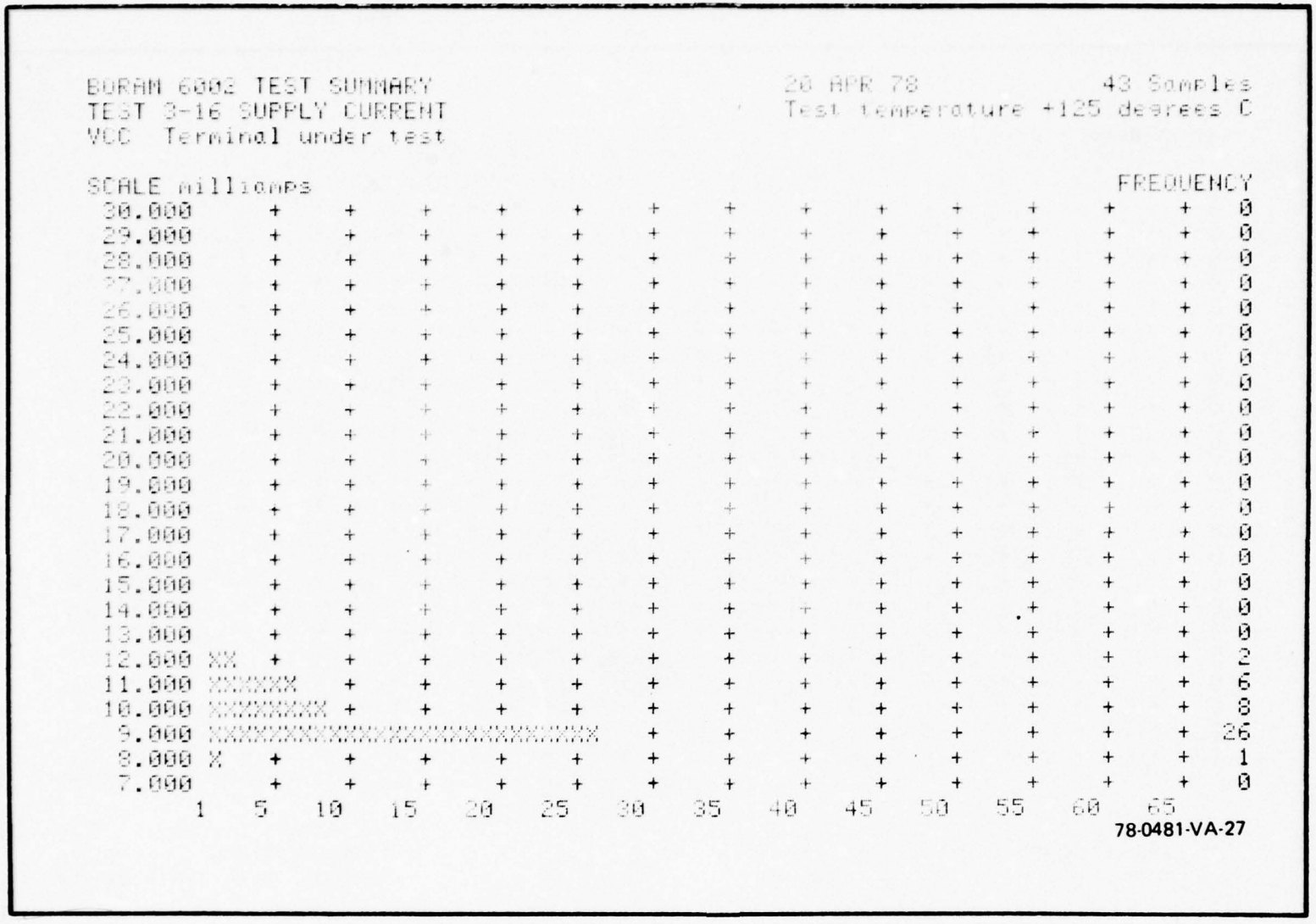

Figure 1-28. Selected Standby Current at 125°C

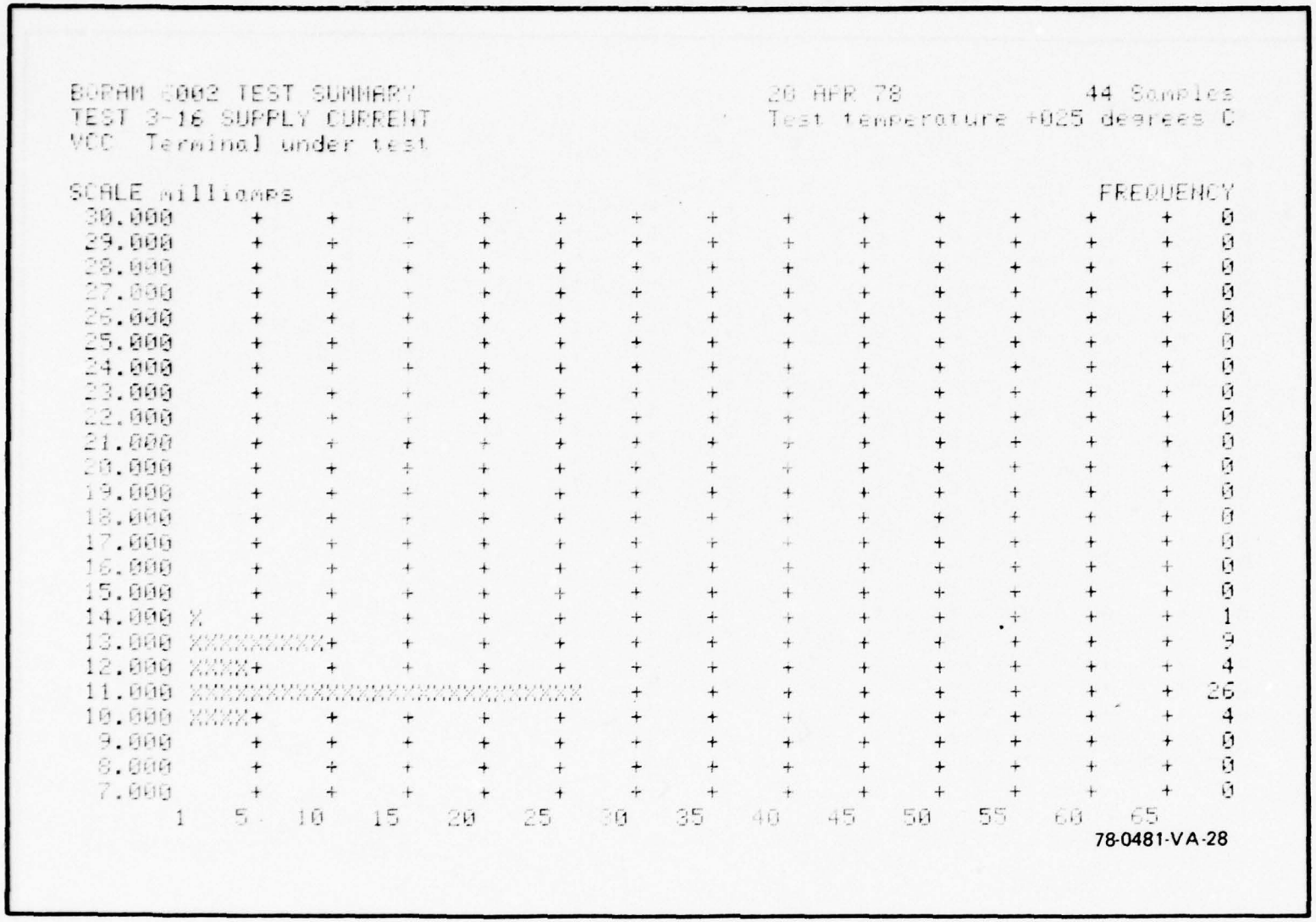

Figure 1-29. Selected Standby Current at 25°C

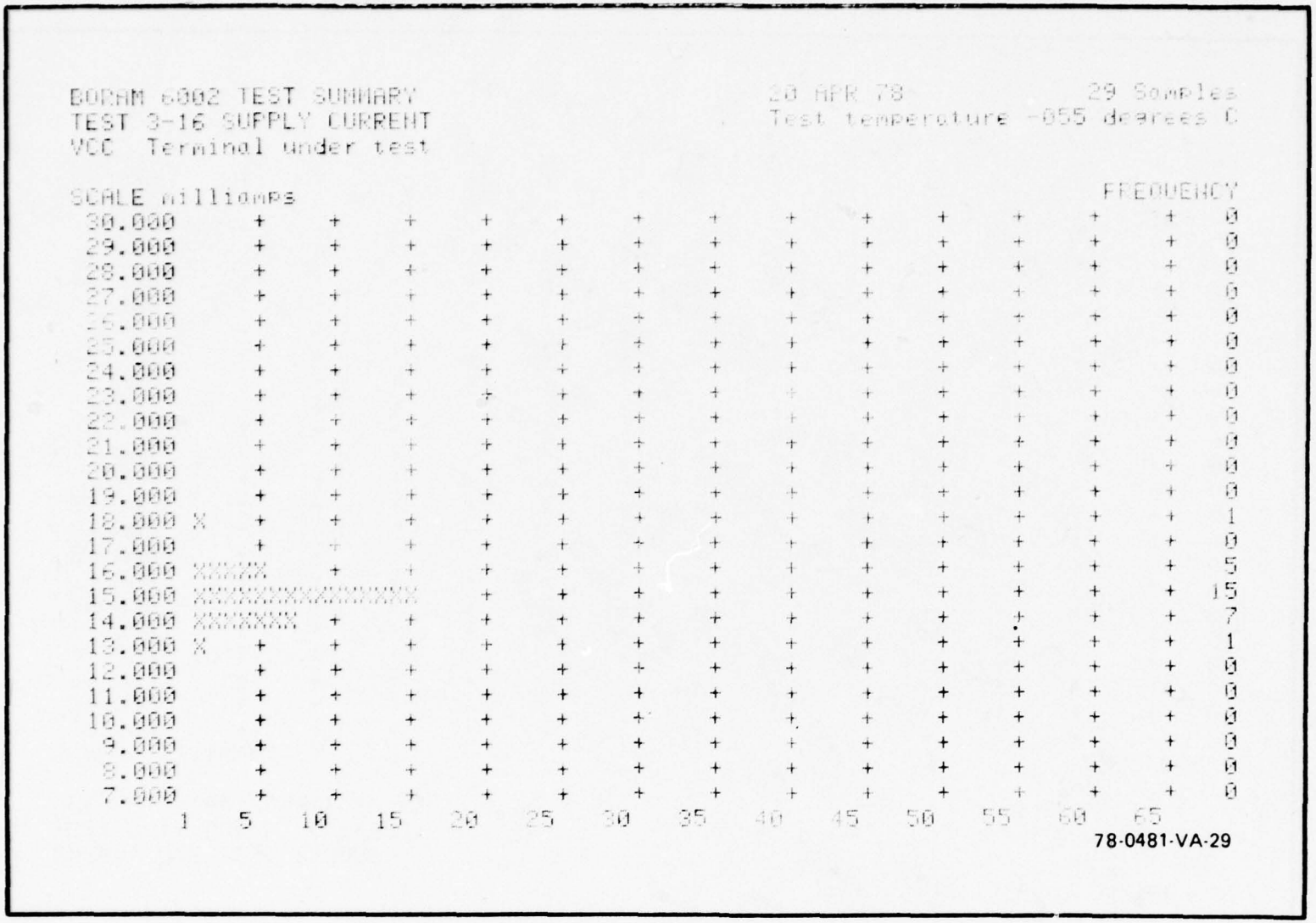

Figure 1-30. Selected Standby Current at -55°C

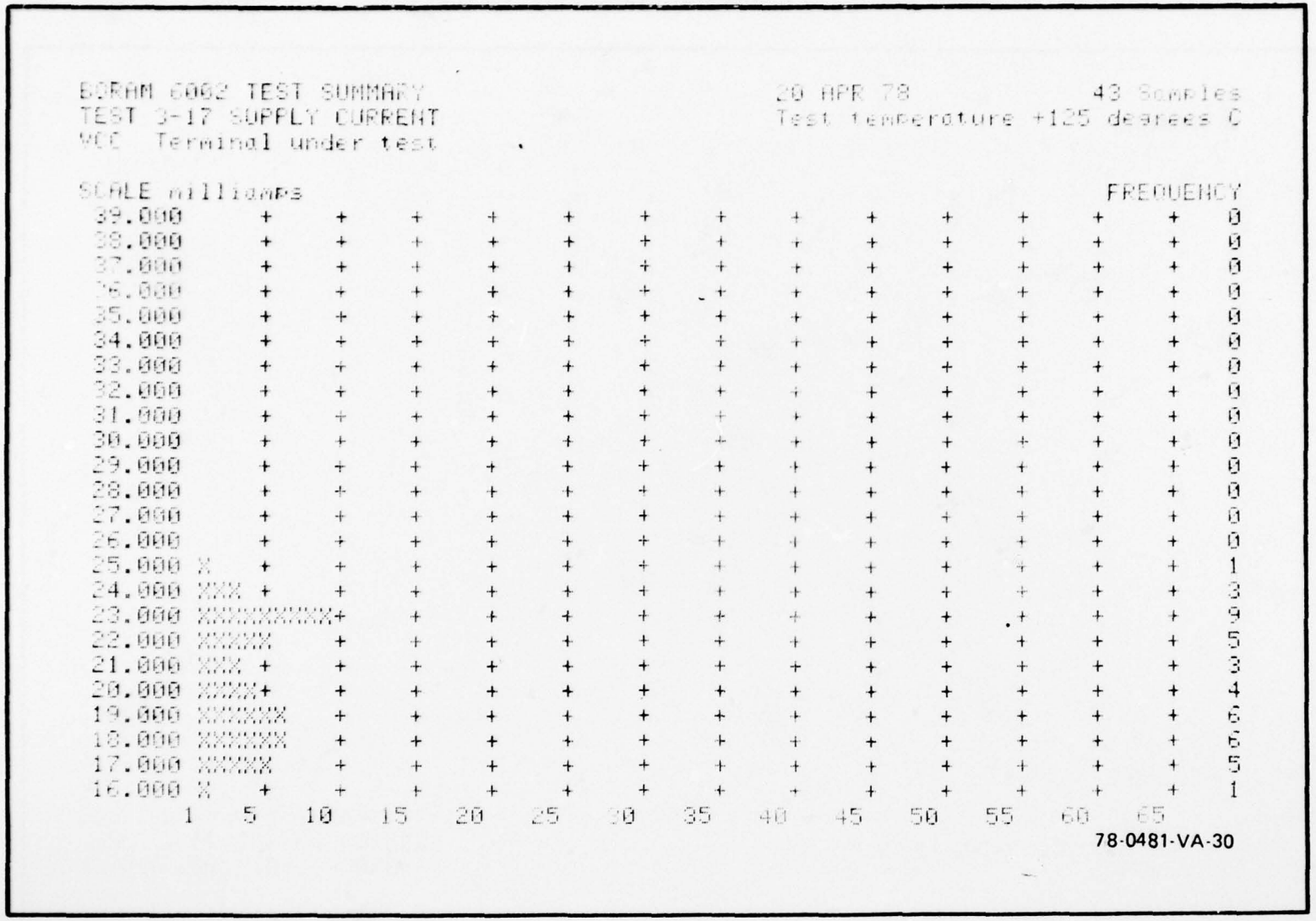

Figure 1-31. Read Current at 125°C

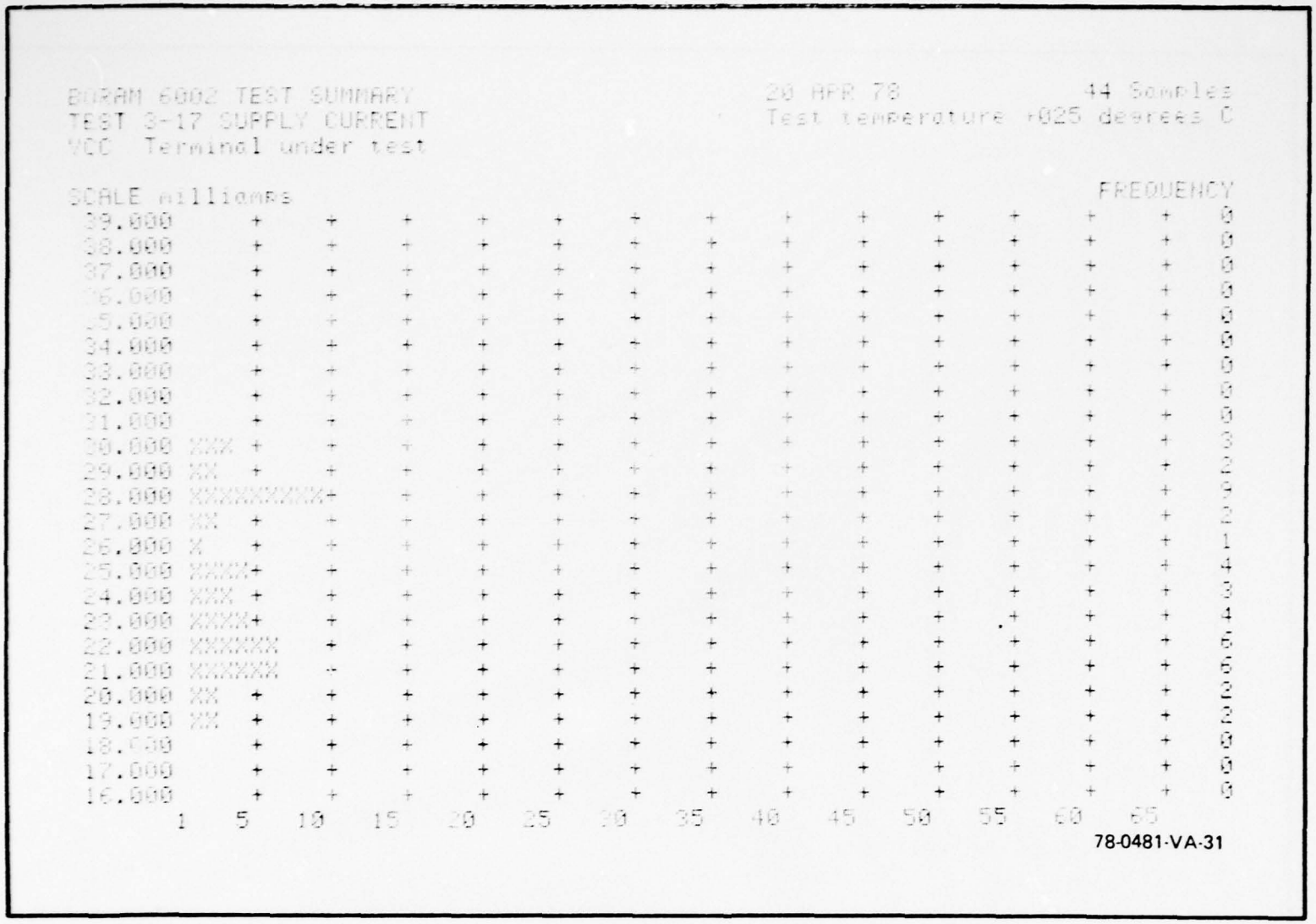

Figure 1-32. Read Current at 25°C

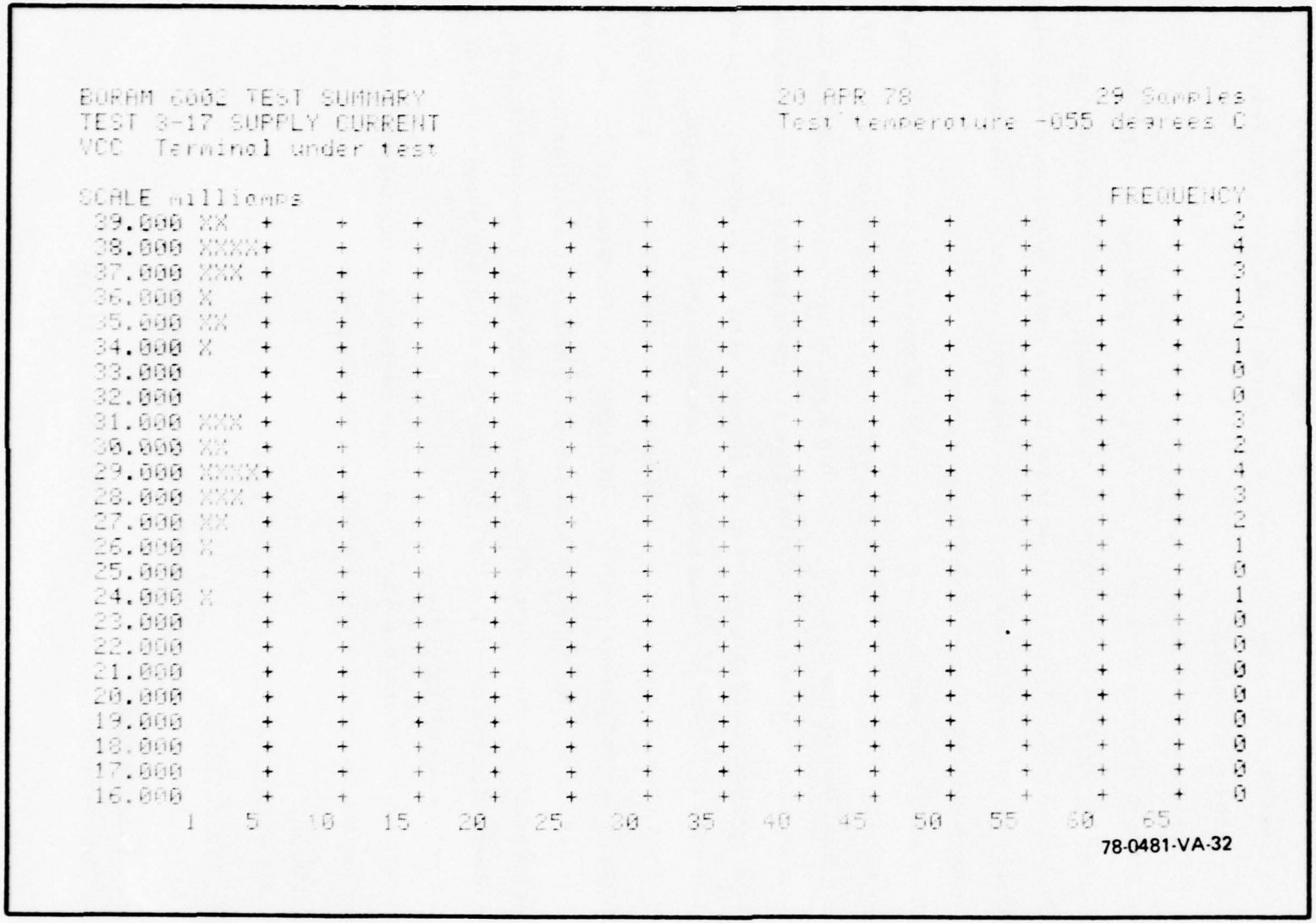

Figure 1-33. Read Current at -55°C

write current appears in figures 1-34, 1-35 and 1-36. Figures 1-37, 1-38 and 1-39 treat the chip clear current, and figures 1-40, 1-41 and 1-42 show the group clear distributions.

1.3.4.2 Operating Mode Power Levels

The subject of power dissipation during circuit operation is relatively complex in that the specific operating mode and detailed timing of control signals must be considered. To clarify this issue the following discussion will relate the supply current levels measured in various static modes to the power dissipation experienced during device operation.

Before static current levels can be related to operating power, it is necessary to establish the specific operating waveform sequences involved. For the electrical test of the BORAM 6002 chip a set of operating conditions have been established. Table 1-21 relates these standard operating conditions to the static currents in terms of the dwell time in each static state. Three operating modes are treated· read mode, block write and group write.

The three operating sequences summarized in table 1-21 were selected to be similar to the conditions called for in Army specification SCS503. In each case, all 2048 bits in the chip are processed. Time is allowed for the device selection and deselection functions. Data is shifted at a 1 megahertz rate. Power dissipation can be computed from the time averaged supply current over the entire operating period.

To compute the average power for a given operating mode the time average current for the operating sequence must be formulated.

READ MODE

IRM = (4IDS+2306ISS+192IR+2048ISR)/2502

BLOCK WRITE MODE

IBW = (4IDS+2435ISS+12800IW+1000ICC+2048ISR)/16239

GROUP WRITE MODE

IGW = (4IDS+2434ISS+12800IW+16000IGC+2048ISR)/31238

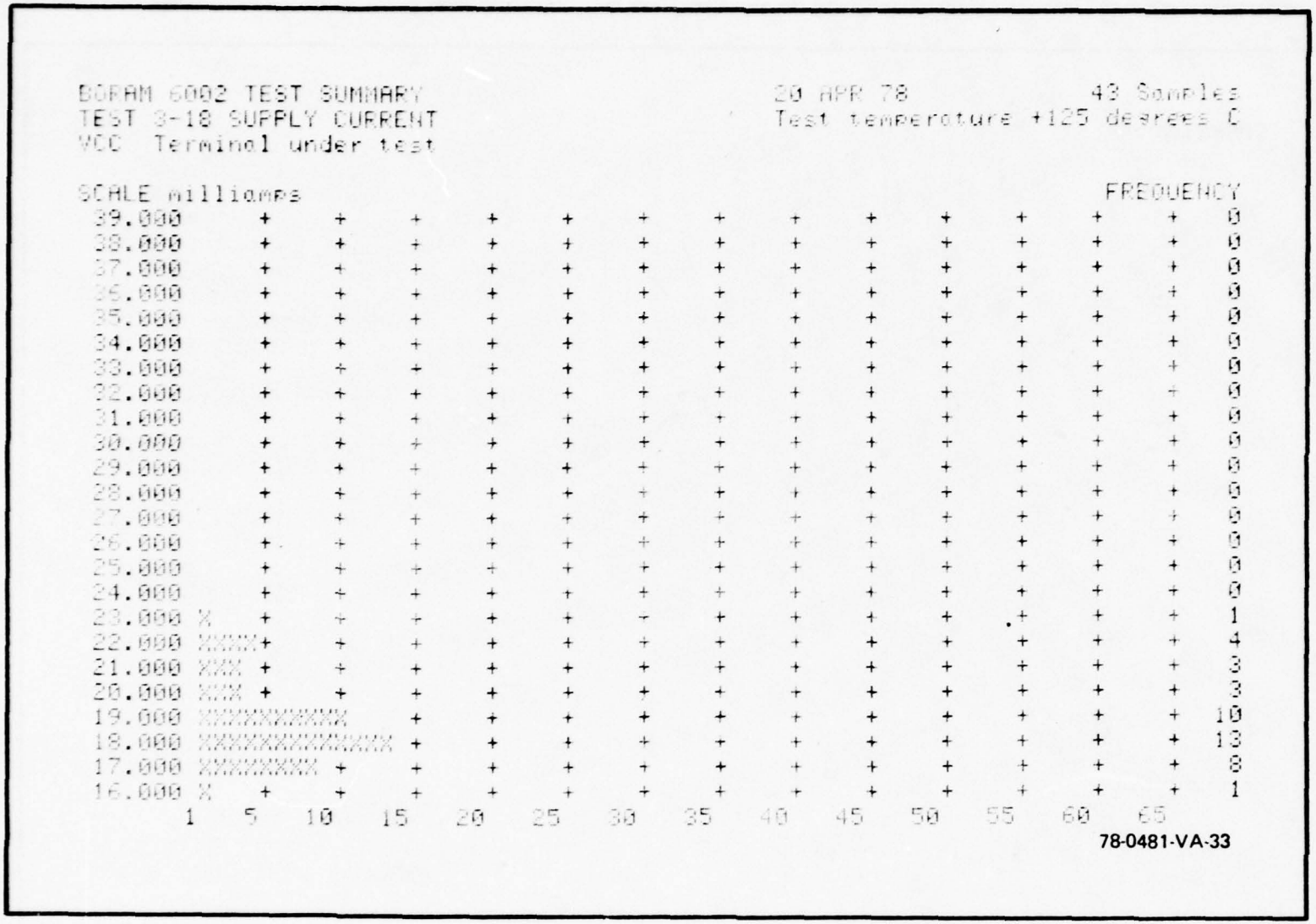

Figure 1-34. Write Current at 125°C

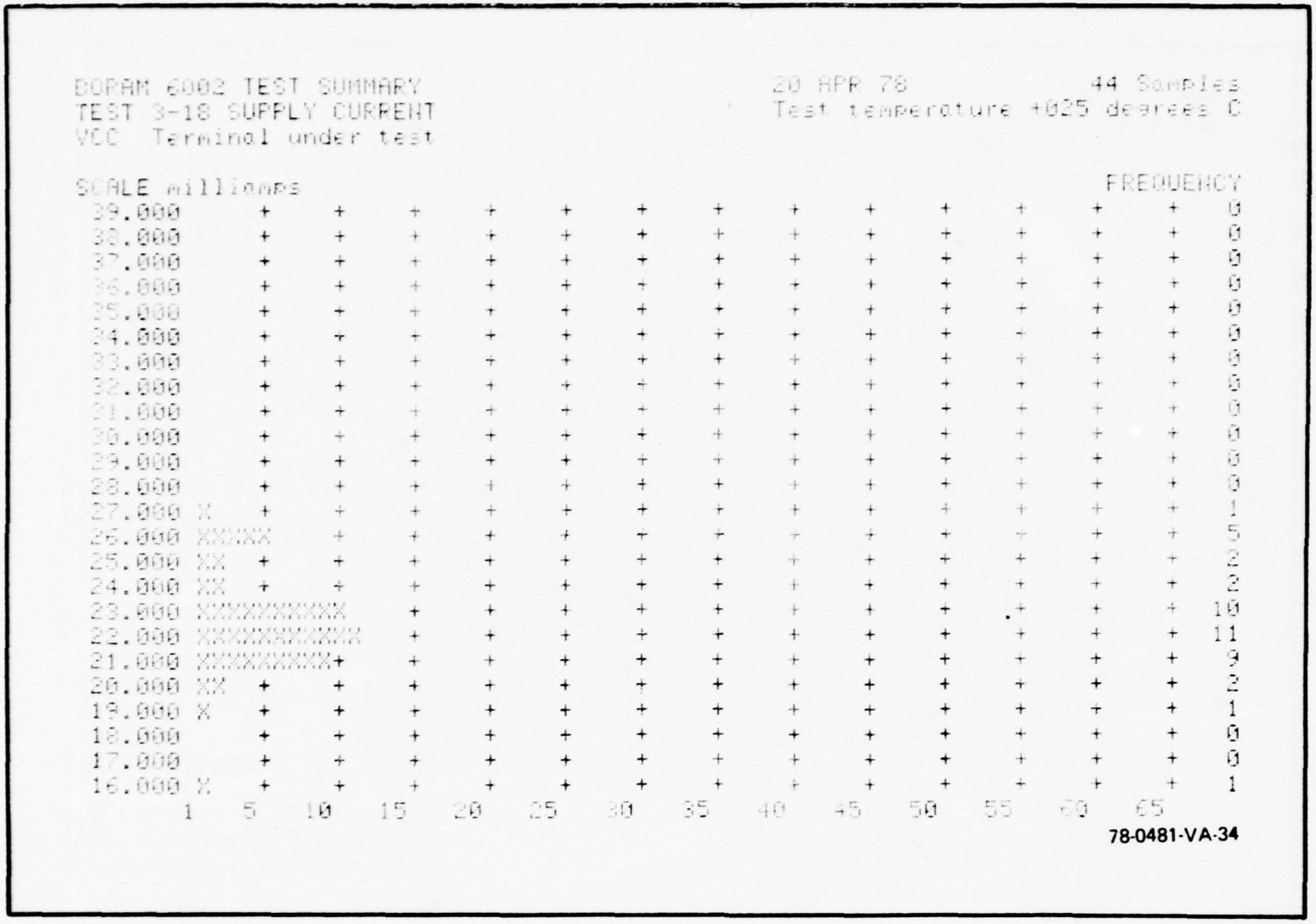

Figure 1-35. Write Current at 25°C

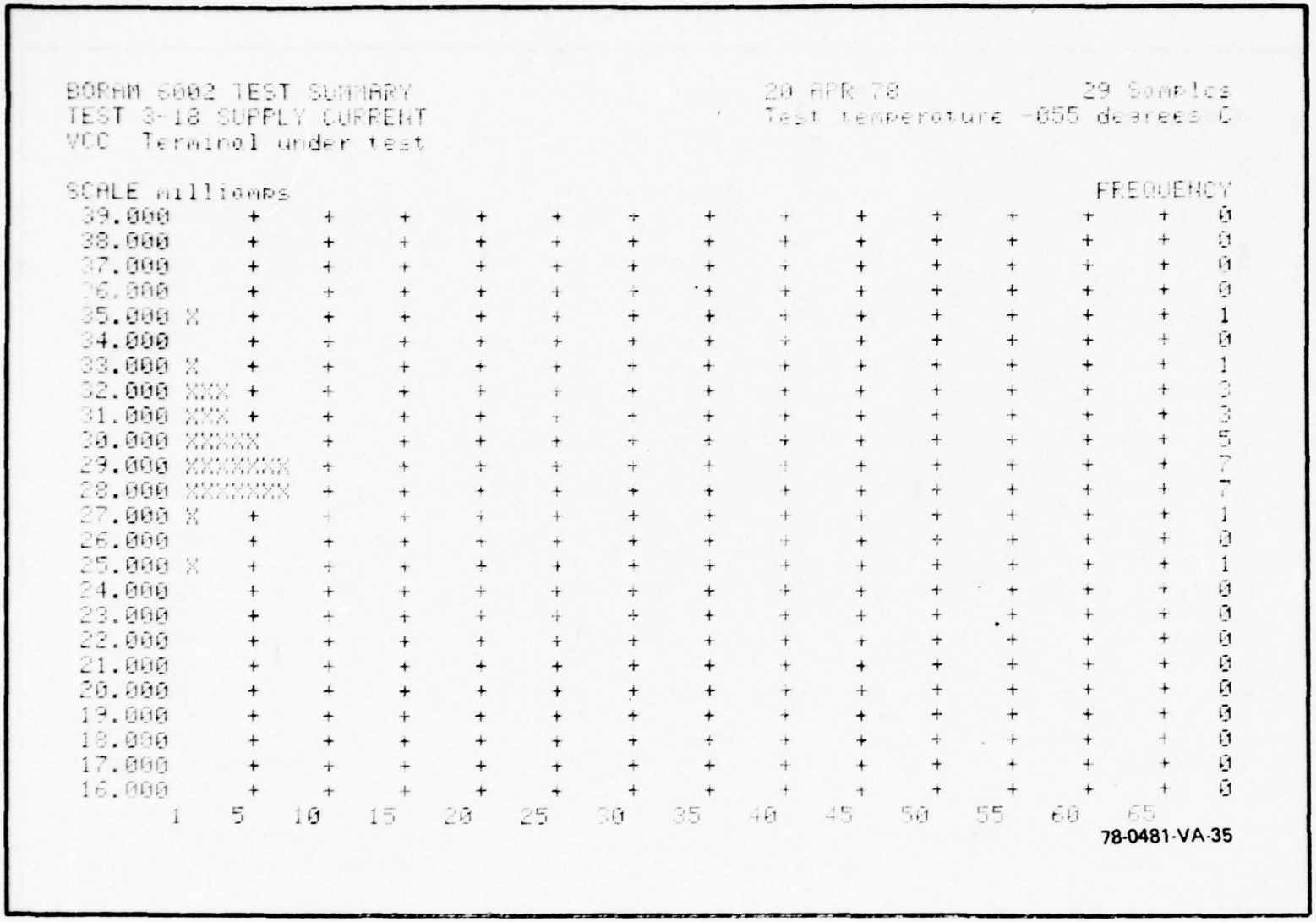

Figure 1-36. Write Current at -55°C

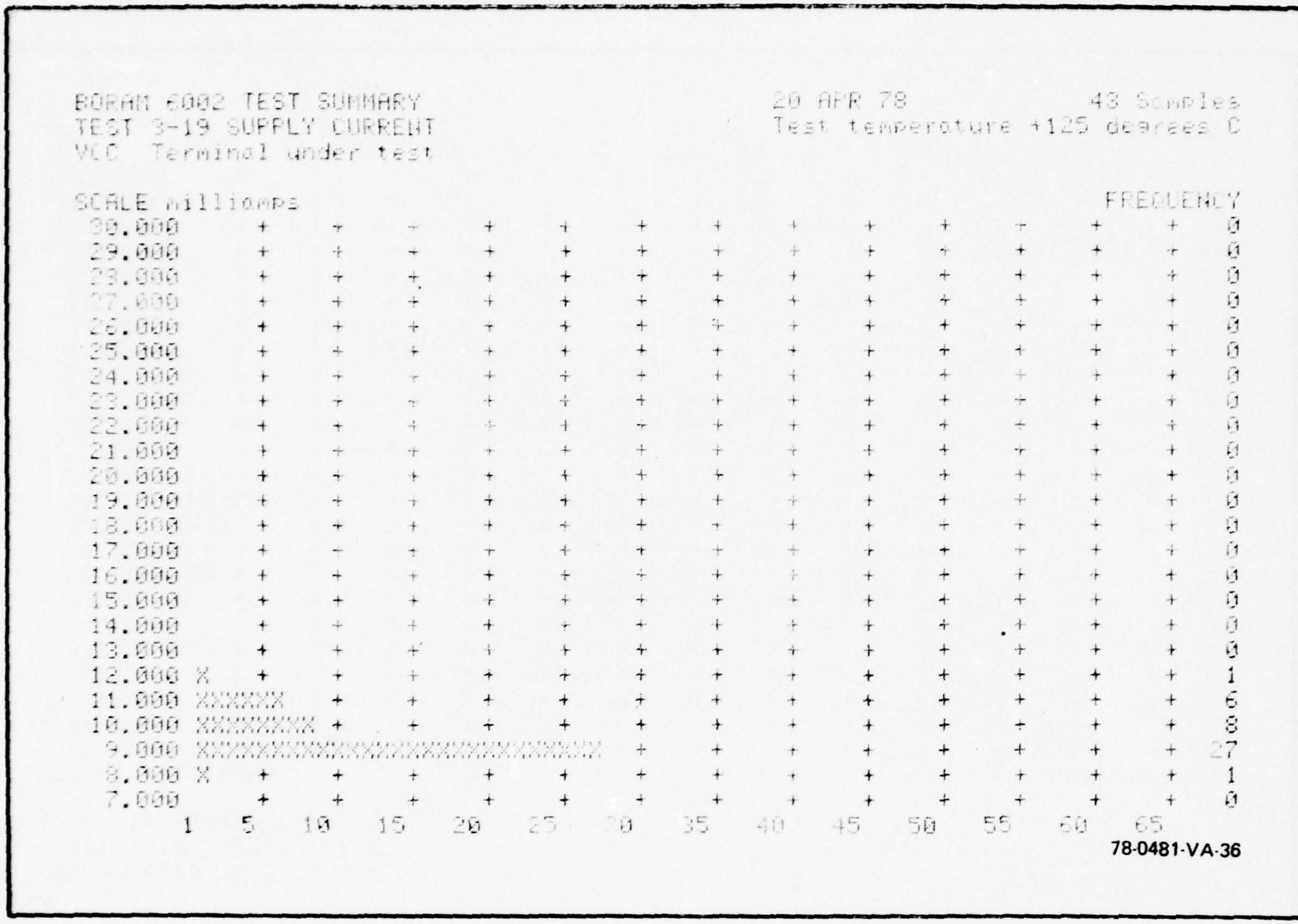

Figure 1-37. Chip Clear Current at 125°C

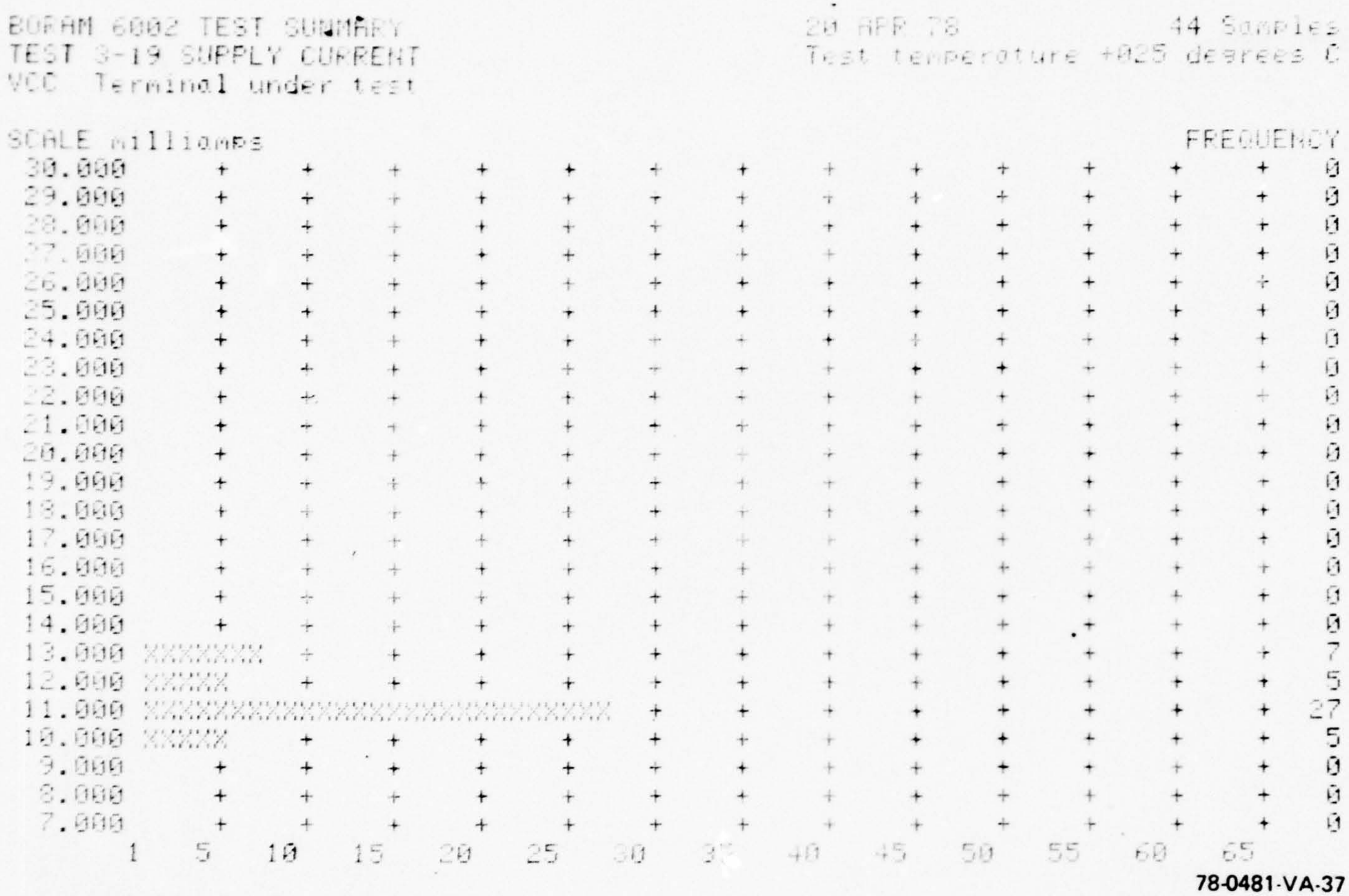

Figure 1-38. Chip Clear Current at 25°C

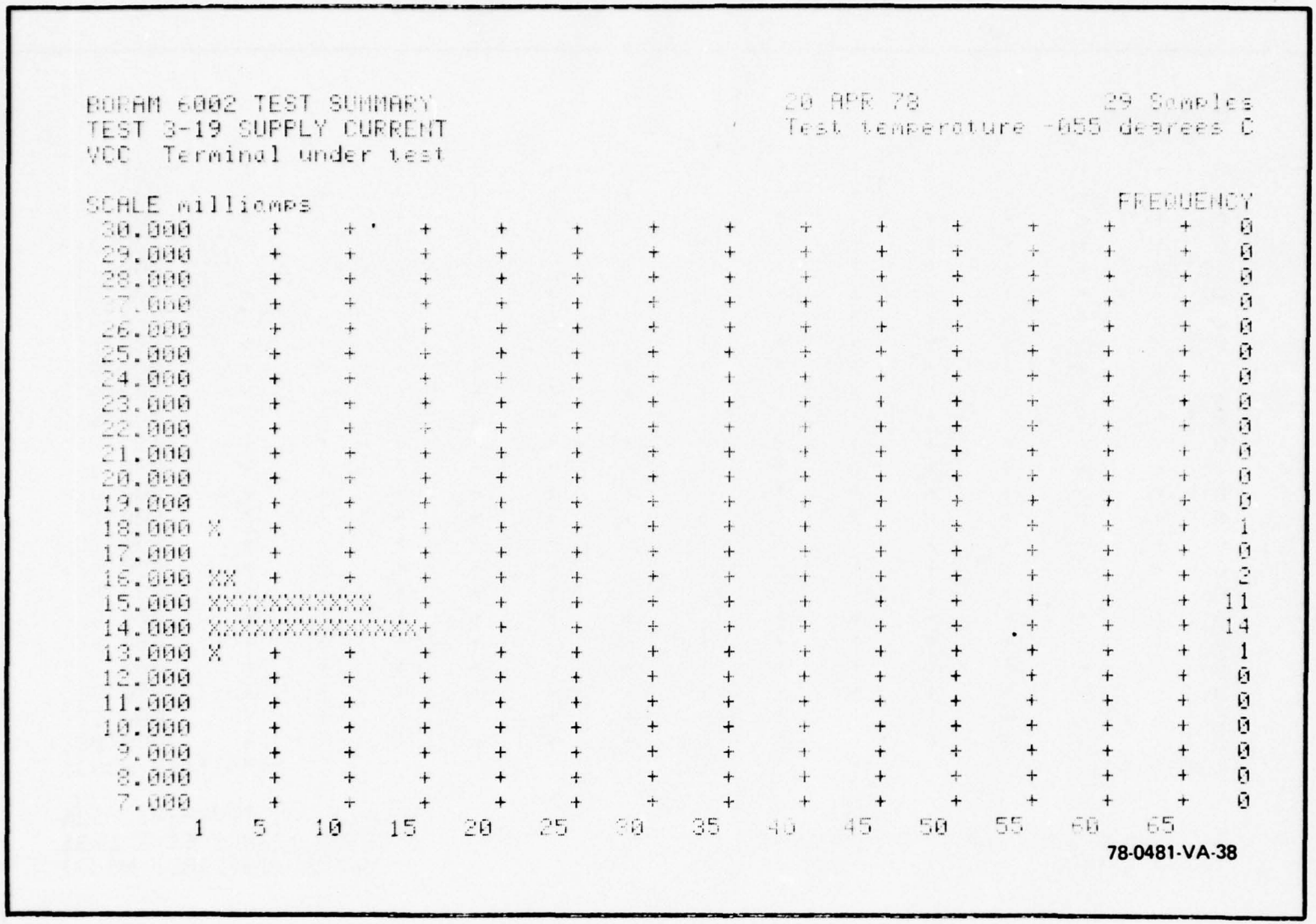

Figure 1-39. Chip Clear Current at -55°C

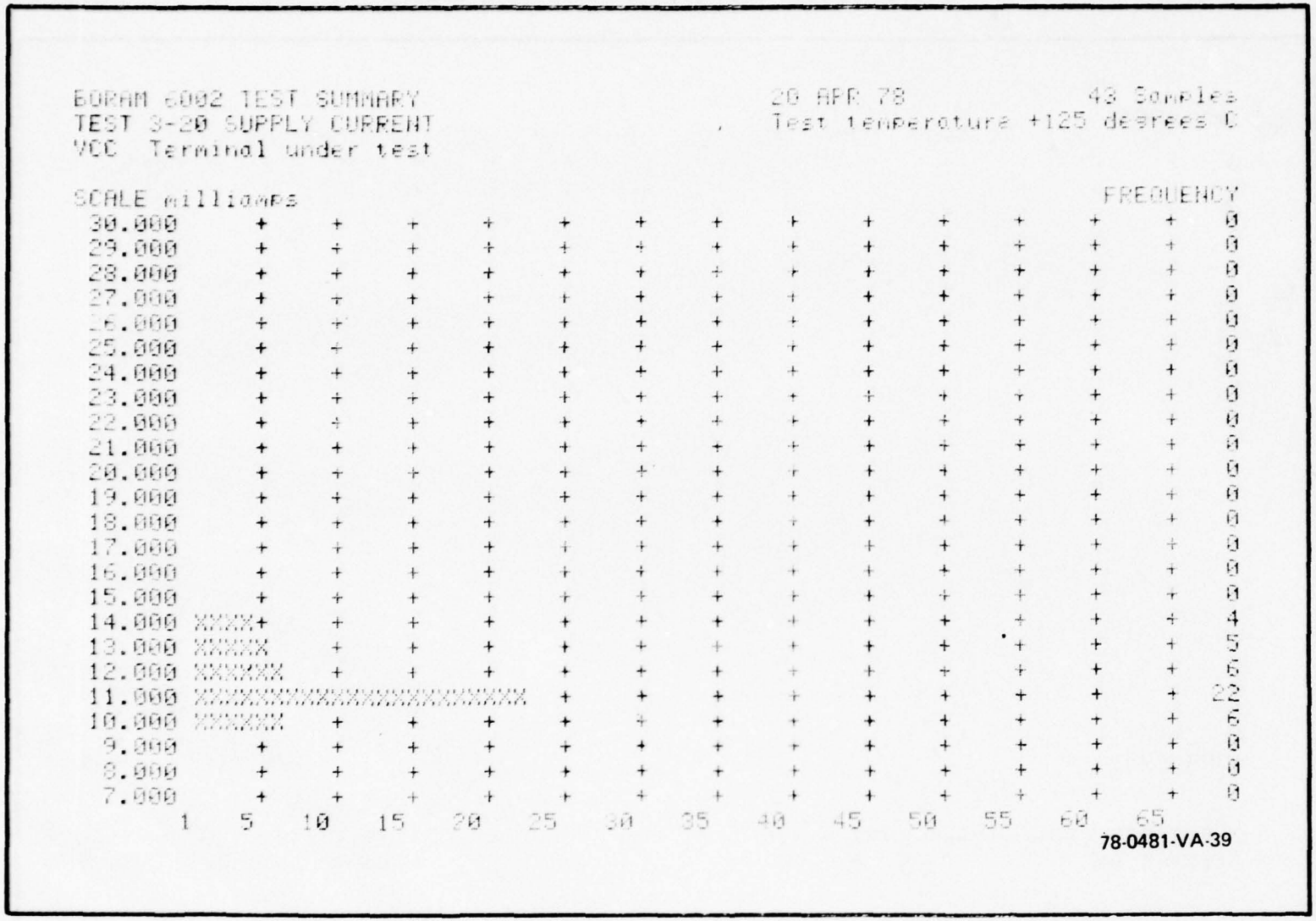

Figure 1-40. Group Clear Current at 125°C

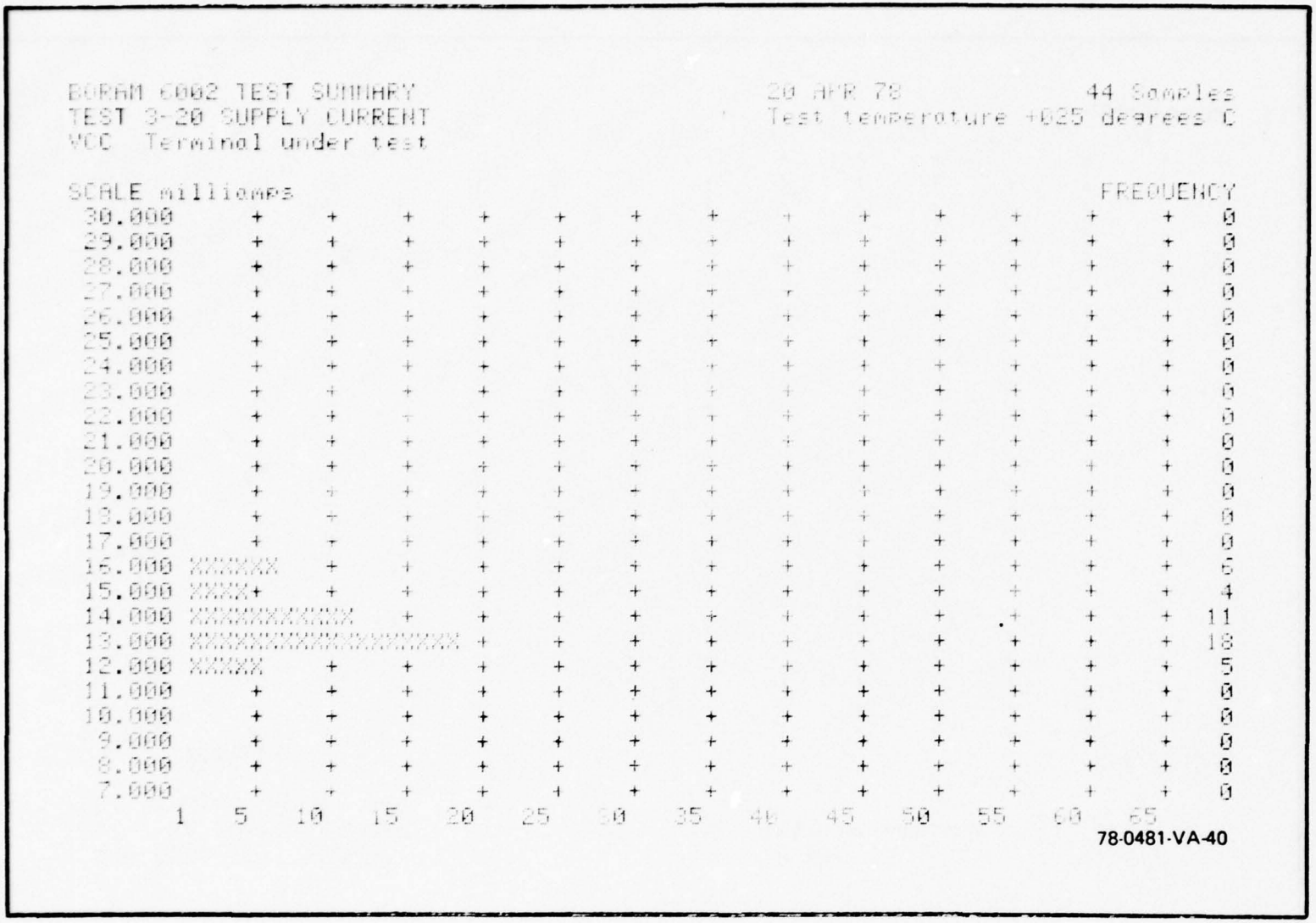

Figure 1-41. Group Clear Current at 25°C

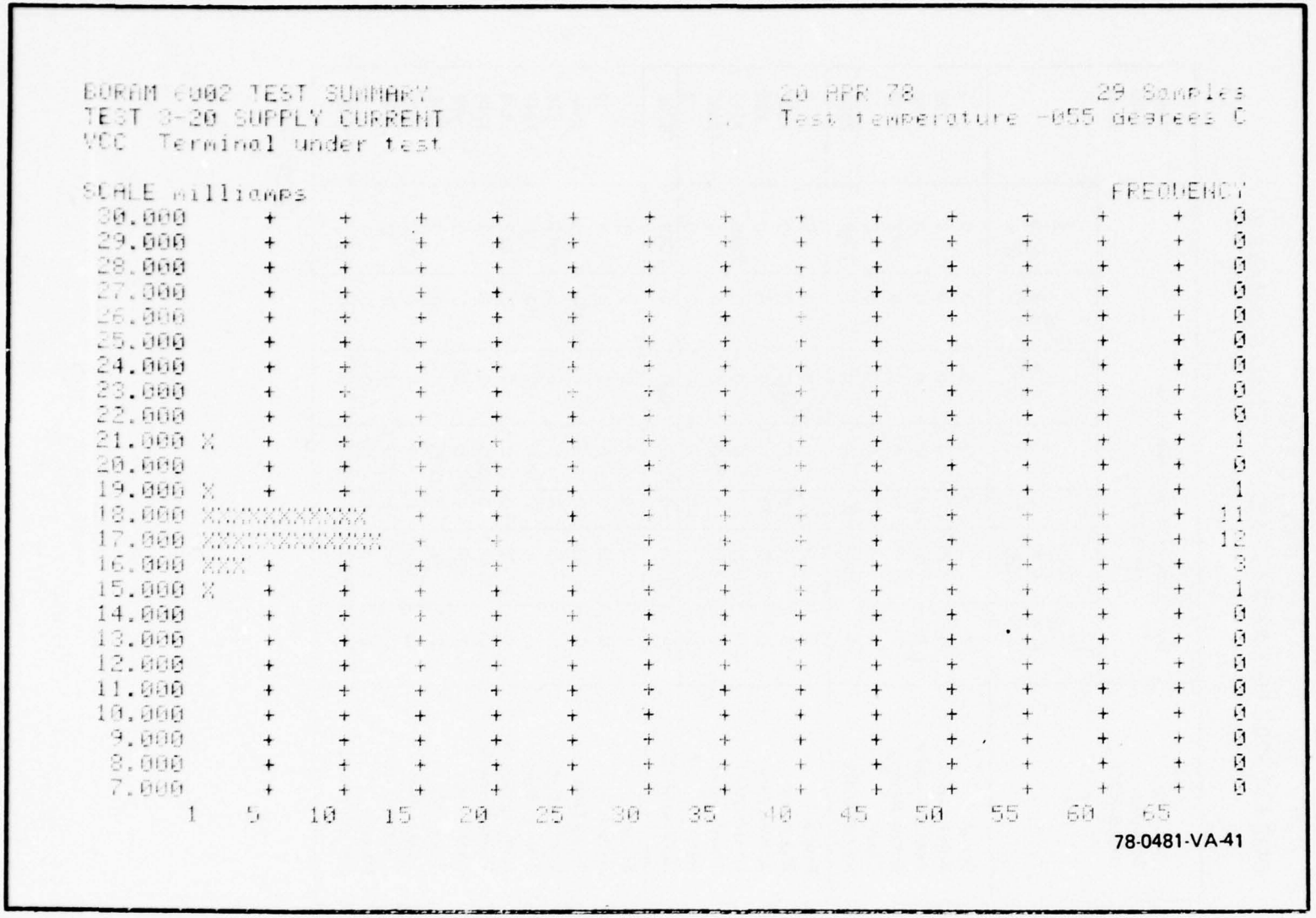

Figure 1-42. Group Clear Current at -55°C

TABLE 1-21
BORAM 6002 OPERATING MODES TIME SUMMARY

Operating Sequence MODE TOTAL	Dwell Time in Static Power States microseconds							Total Time μsec
	Preselected Standby	Selected Standby	Read	Write	Chip Clear	Group Clear	Shift Register	
Set-up	2	1	0	0	0	0	0	3
Address latch	0	128	0	0	0	0	0	128
Read & Transfer	0	64	192	0	0	0	0	256
Empty Register	0	2112	0	0	0	0	2048	2112
Reset	2	1	0	0	0	0	0	3
READ MODE	4	2306	192	0	0	0	2048	2502
Set-up	2	1	0	0	0	0	0	3
Block erase	0	1	0	0	1000	0	0	1001
Address latch	0	128	0	0	0	0	0	128
Load register	0	2112	0	0	0	0	2048	2112
Transfer & write	0	192	0	12800	0	0	0	12992
Reset	2	1	0	0	0	0	0	3
BLOCK WRITE	4	2435	0	12800	1000	0	2048	16239
Set-up	2	1	0	0	0	0	0	3
Address latch	0	32	0	0	0	0	0	32
Group erase	0	96	0	0	0	16000	0	16096
Load register	0	528	0	0	0	0	512	528
Transfer & write	0	48	0	3200	0	0	0	3248
Load register	0	528	0	0	0	0	512	528
Transfer & write	0	48	0	3200	0	0	0	3248
Load register	0	528	0	0	0	0	0	528
Transfer & write	0	48	0	3200	0	0	0	3248
Load register	0	528	0	0	0	0	512	528
Transfer & write	0	48	0	3200	0	0	0	3248
Reset	2	1	0	0	0	0	0	3
GROUP WRITE	4	2434	0	12800	0	16000	2048	31238

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The respective power levels at a nominal VCC to VGG voltage of 30 volts would be

PRM = 30IRM PBW = 30IBW PGW = 30IGW

A computer program was written to accept the static current values given in table 1-19 and use the average current equations to compute power. The results are listed in table 1-22.

1.4 TEST STRUCTURE OBSERVATIONS

A series of five measurements in the characterization program are made on nodes that are not normally accessible after packaging. Table 1-23 presents the mean values obtained from sample populations at 125°C, 25°C and -55°C.

This information was obtained from subsets of the samples used for the integrated circuit data presented earlier in this report. The computer data reduction program was used to eliminate grossly defective samples from the populations.

TABLE 1-22
BORAM 6002 OPERATING POWER LEVELS

Operating Mode	Average Power Dissipation		
	$-55^{o}C$ mW	$25^{o}C$ mW	$125^{o}C$ mW
READ	504.2	382.3	316.5
BLOCK WRITE	783.0	593.1	496.0
GROUP WRITE	653.3	501.2	419.0

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TABLE 1-23
OBSERVED TEST STRUCTURE CHARACTERISTICS

Measured Parameter	Observed Mean Voltage			Temperature Sensitivity	
	−55°C Volts	25°C Volts	125°C Volts	V(−55)/V(25) Numeric	V(125)/V(25) Numeric
Nonmemory Transistor Threshold	−2.462	−2.395	−2.333	1.028	0.974
Memory Transistor High Conduction Threshold	−2.493	−2.467	−2.430	1.011	0.985
Memory Transistor Low Conduction Threshold	−13.107	−13.032	−12.732	1.006	0.977
Memory Substrate Voltage High	−4.083	−3.500	−2.176	1.168	0.622
Memory Substrate Voltage Low	−25.583	−26.068	−26.033	0.981	0.999

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Figures 1-46 to 148 show the distribution of nonmemory transistor threshold voltages. The distribution of memory transistor high conduction thresholds are shown in figures 1-49, 1-50 and 1-51; and low conduction thresholds are shown in figures 1-52, 1-53 and 1-54. The high voltage level of the memory substrate is displayed in figures 1-52, 1-53 and 1-54. Memory substrate low voltages during erase are shown in figures 1-55 to 1-57.

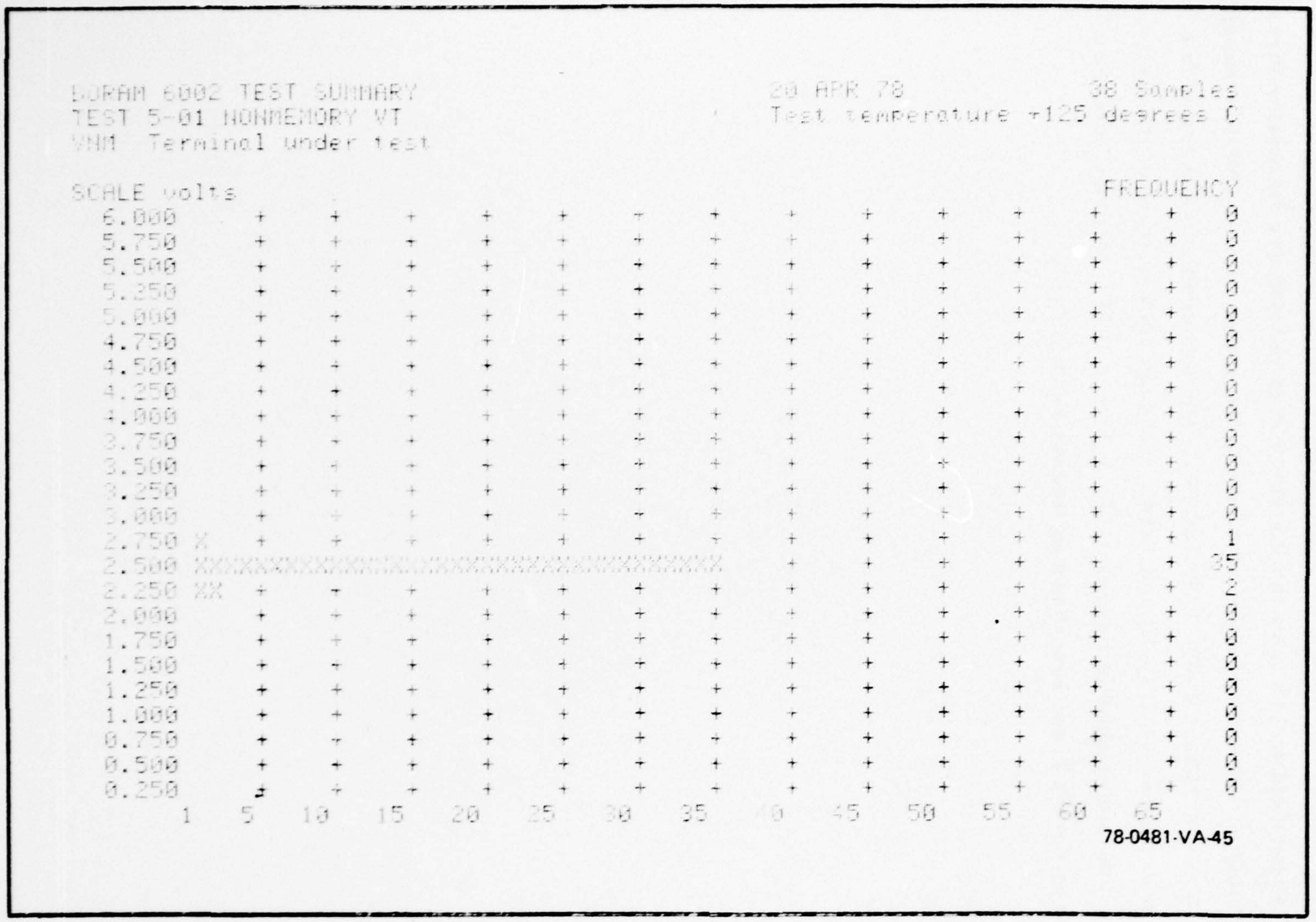

Figure 1-43. Nonmemory Transistor Threshold at 125°C

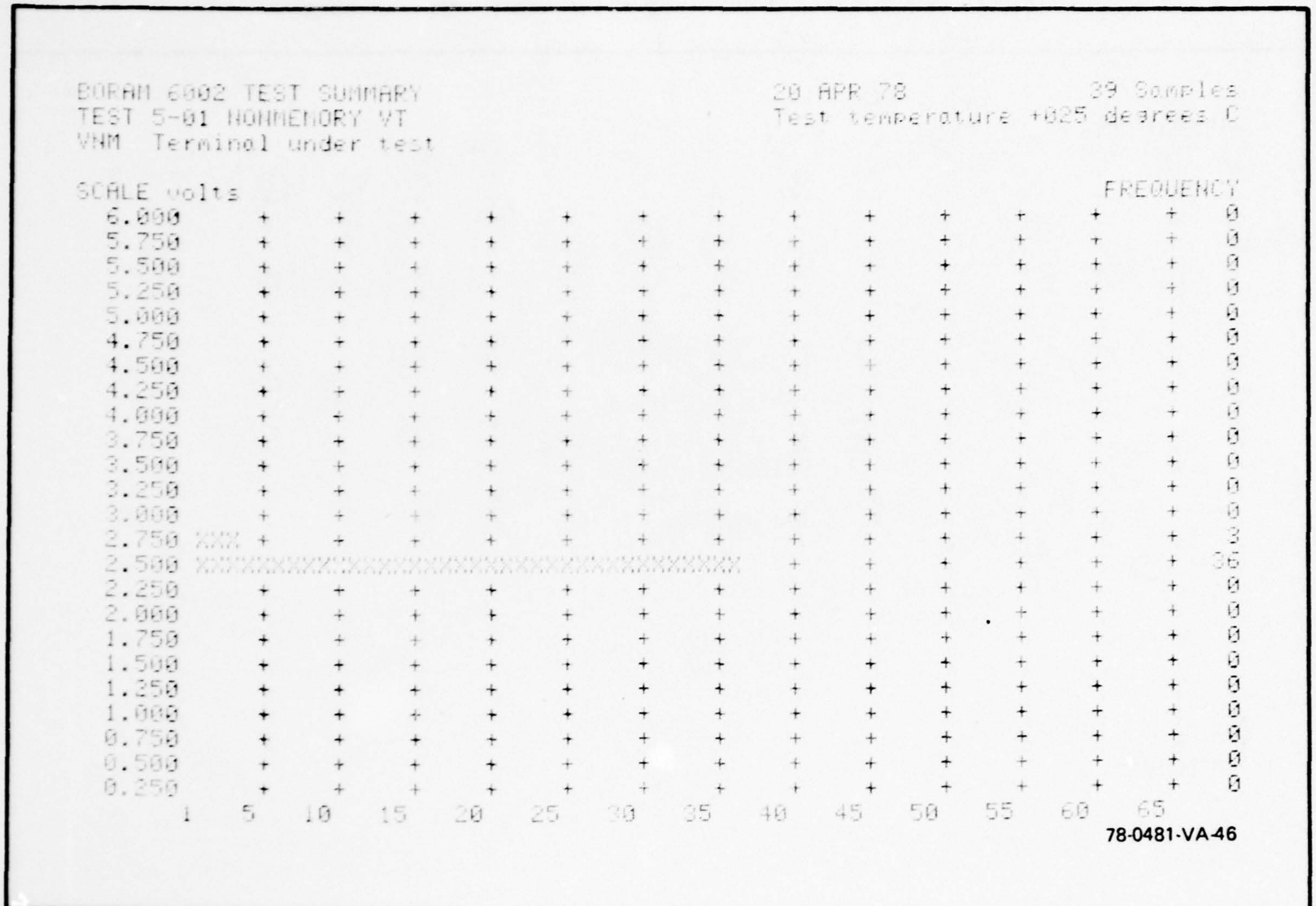

Figure 1-44. Nonmemory Transistor Threshold at 25°C

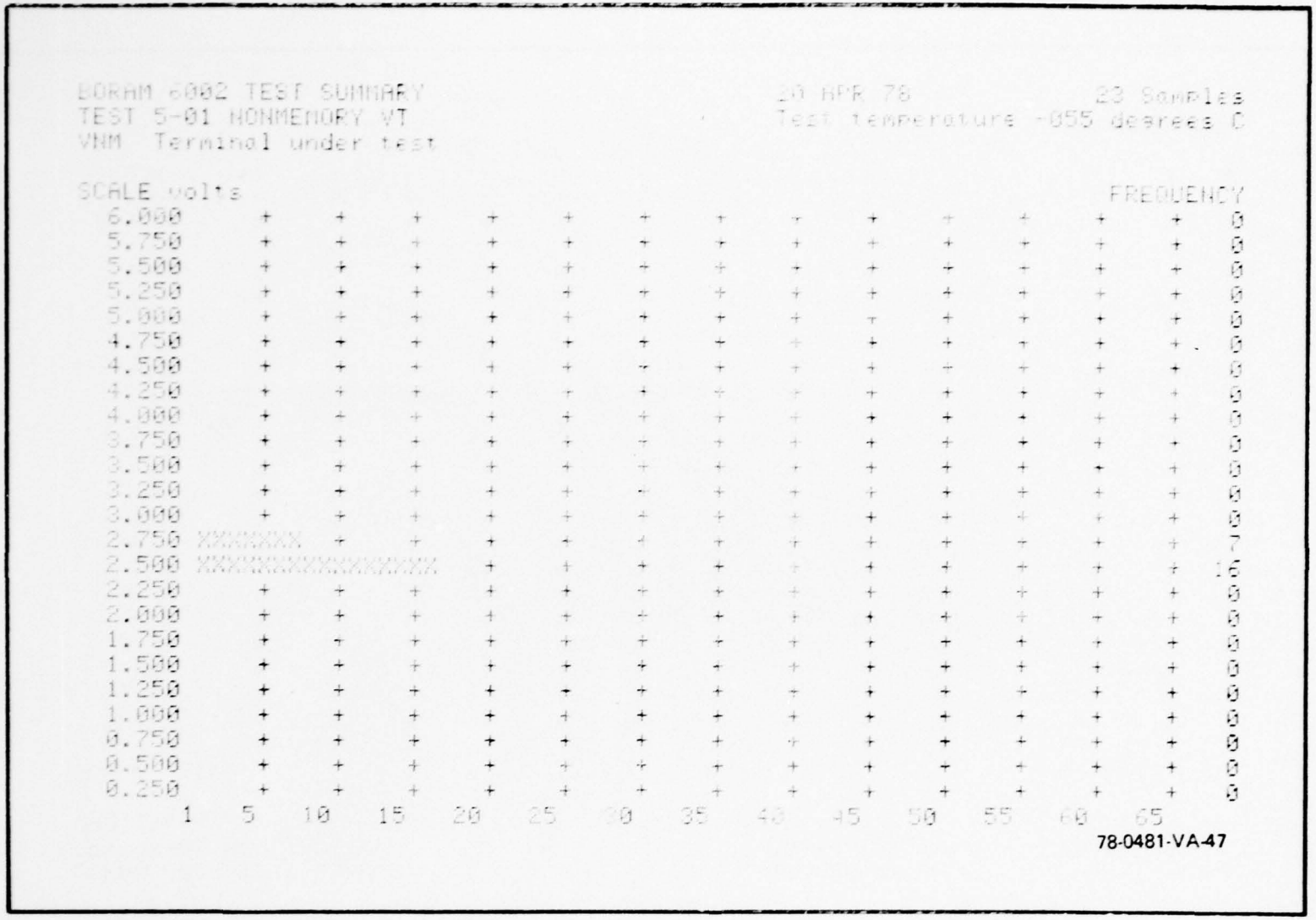

Figure 1-45. Nonmemory Transistor Threshold at -55°C

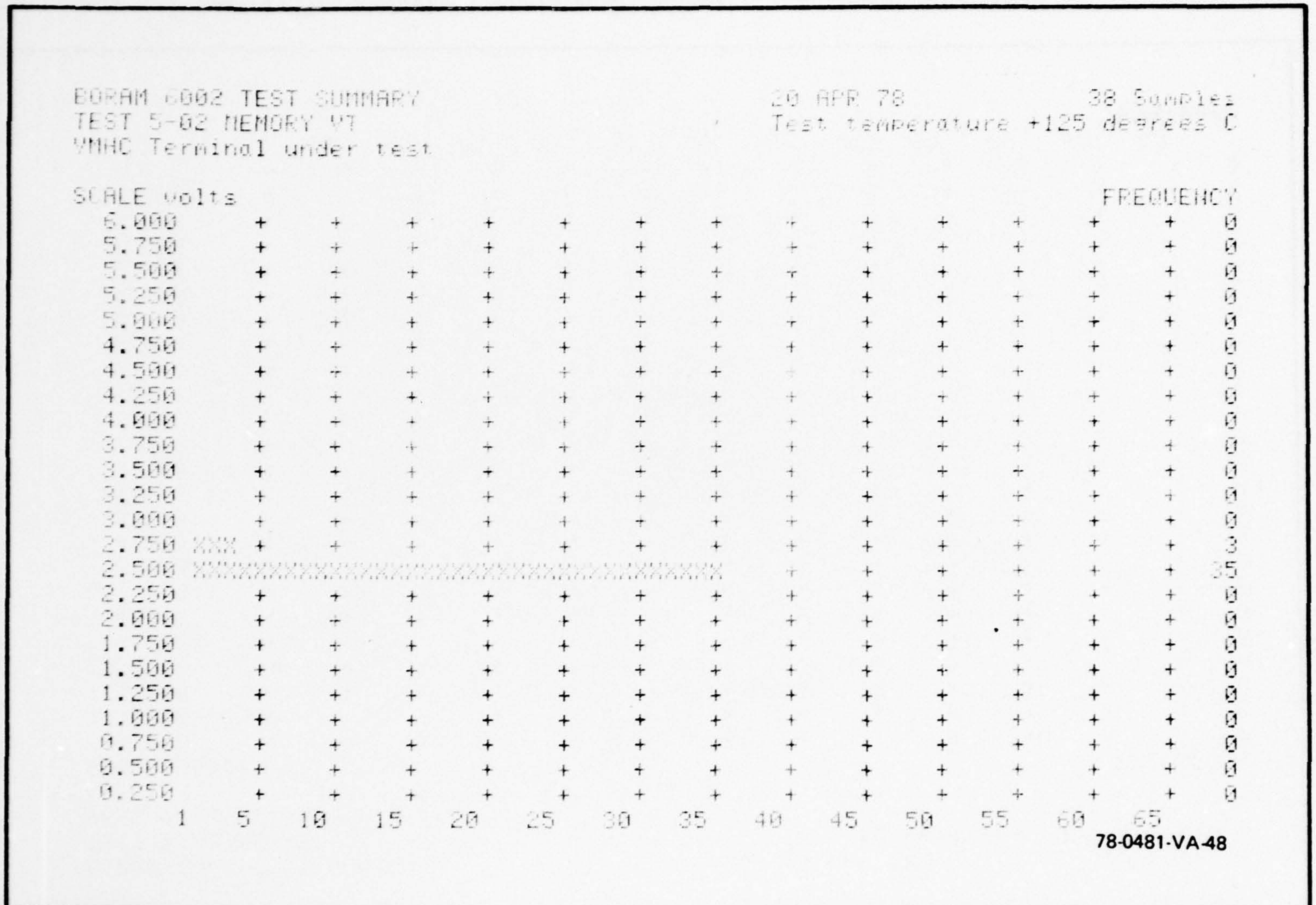

Figure 1-46. Memory Transistor High Conduction Threshold at 125°C

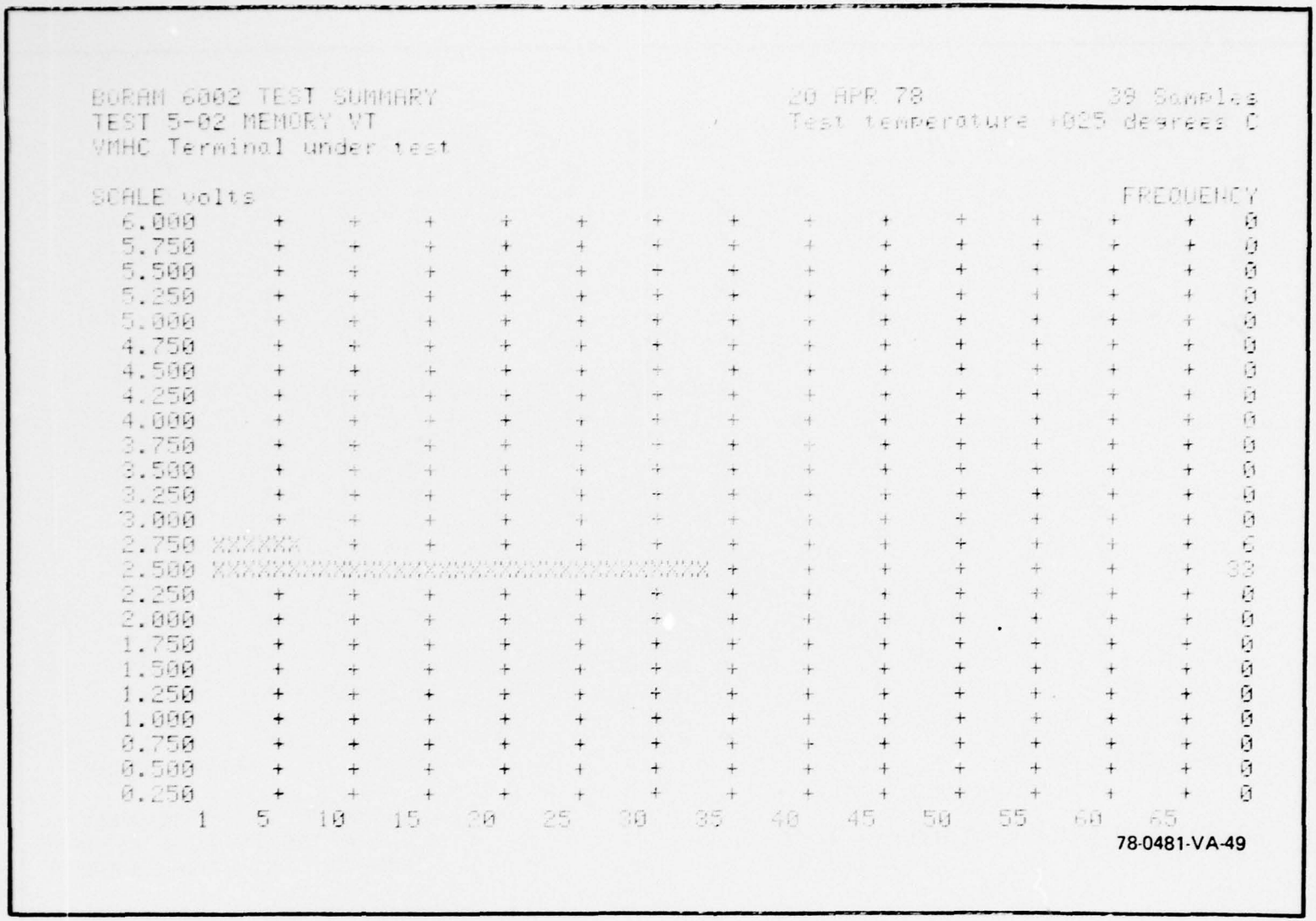

Figure 1-47. Memory Transistor High Conduction Threshold at 25°C

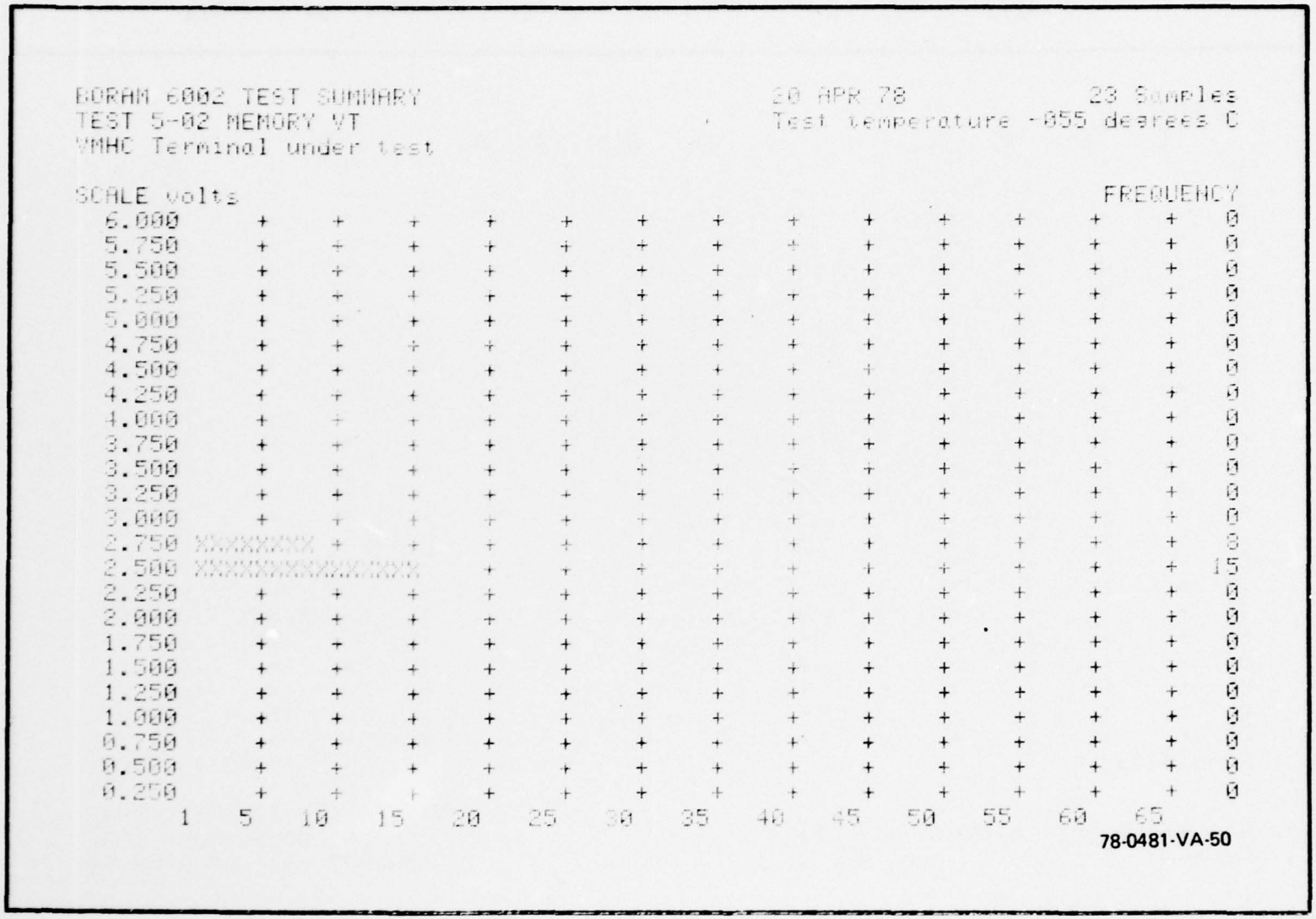

Figure 1-48. Memory Transistor High Conduction Threshold at -55°C

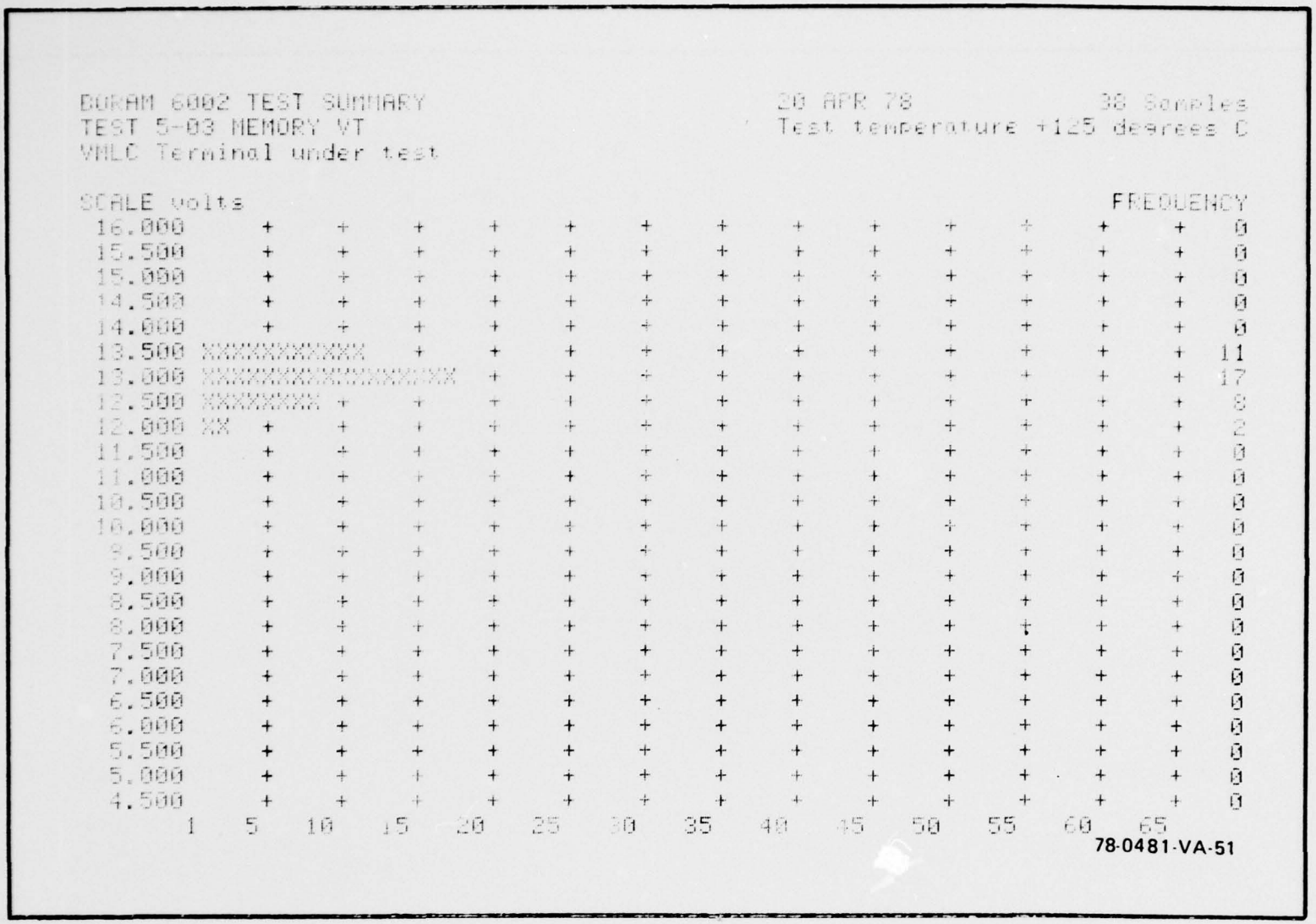

Figure 1-49. Memory Transistor Low Conduction Threshold at 125°C

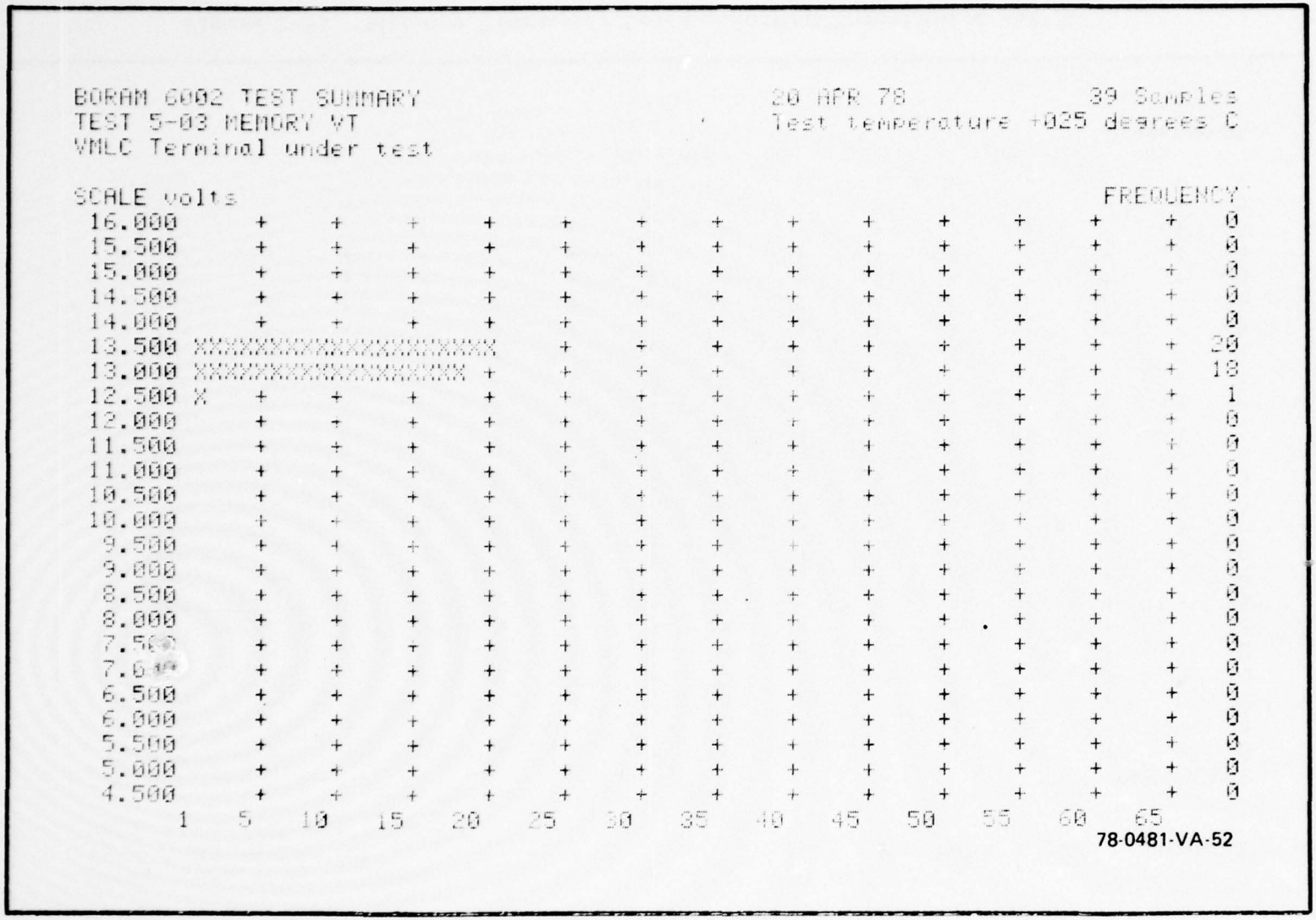

Figure 1-50. Memory Transistor Low Conduction Threshold at 25°C

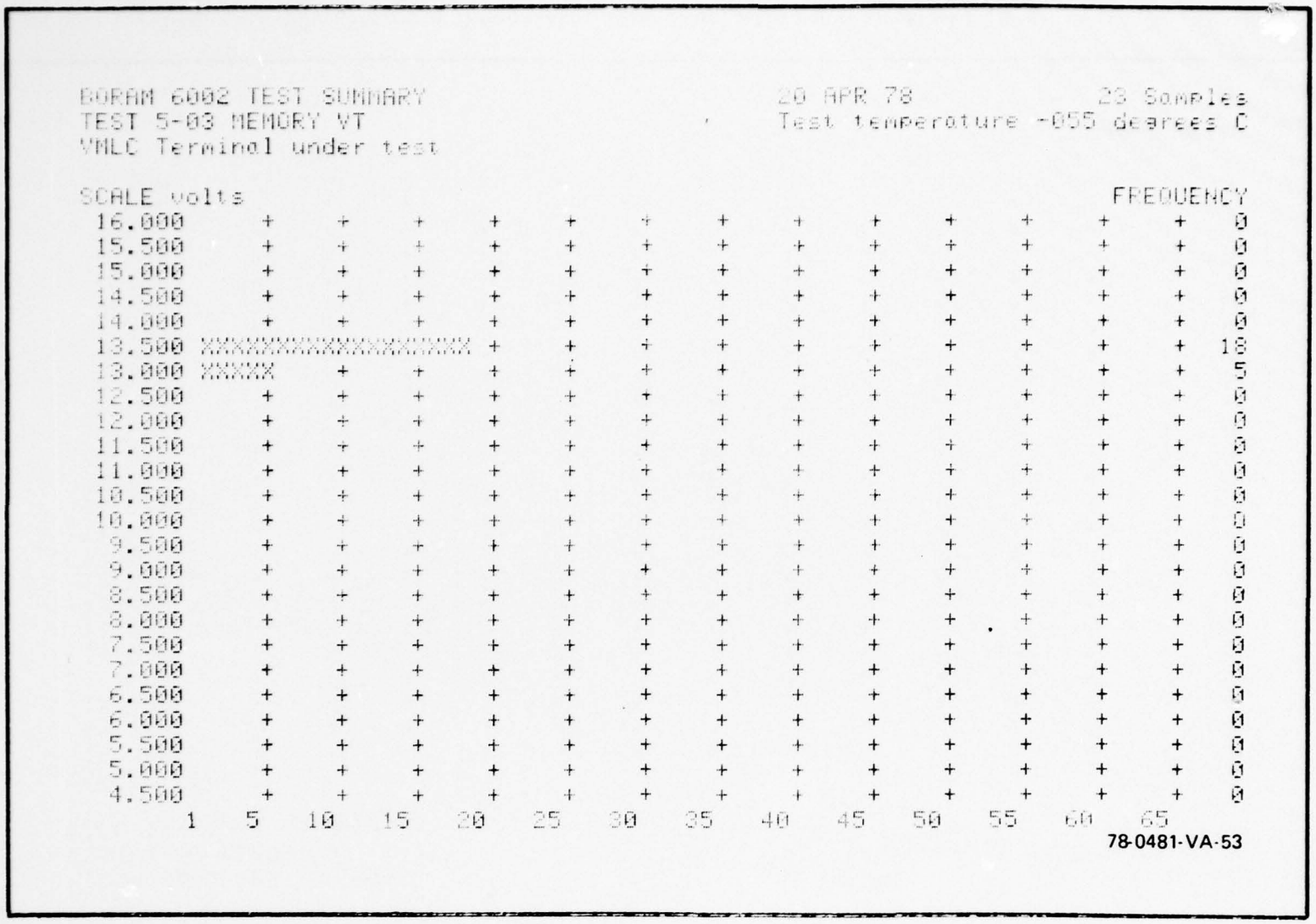

Figure 1-51. Memory Transistor Low Conduction Threshold at -55°C

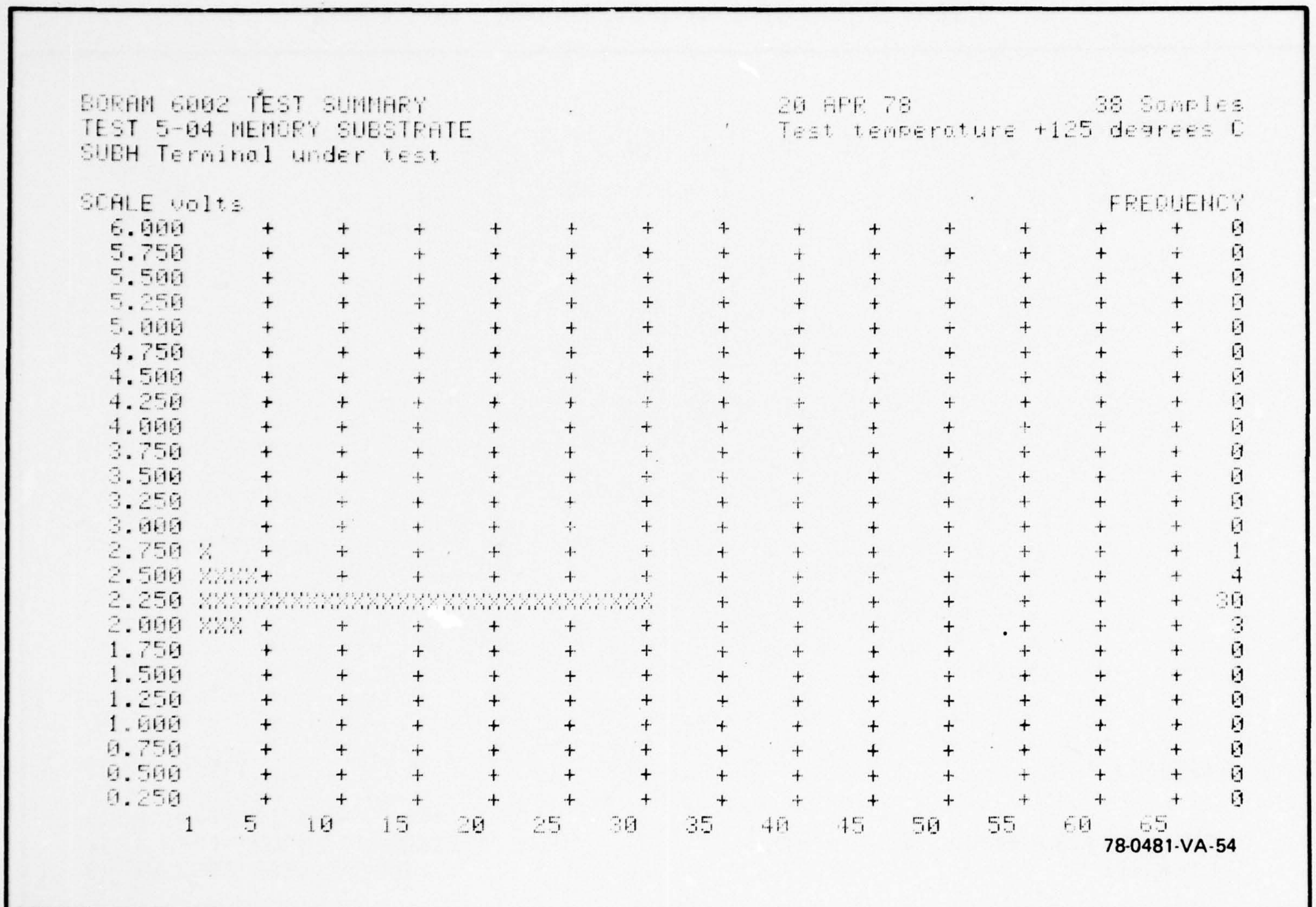

Figure 1-52. Memory Substrate Voltage High at 125°C

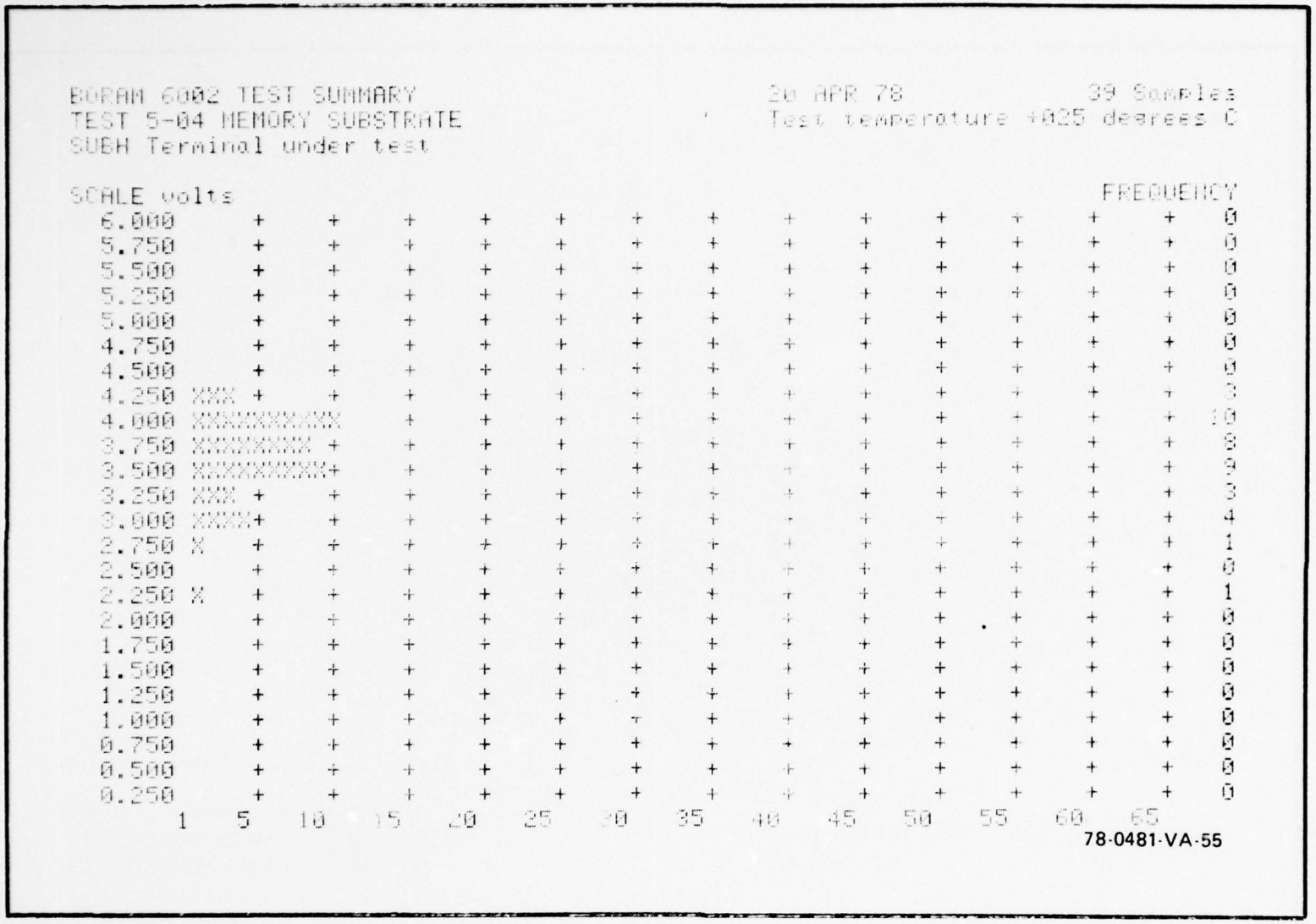

Figure 1-53. Memory Substrate Voltage High at 25°C

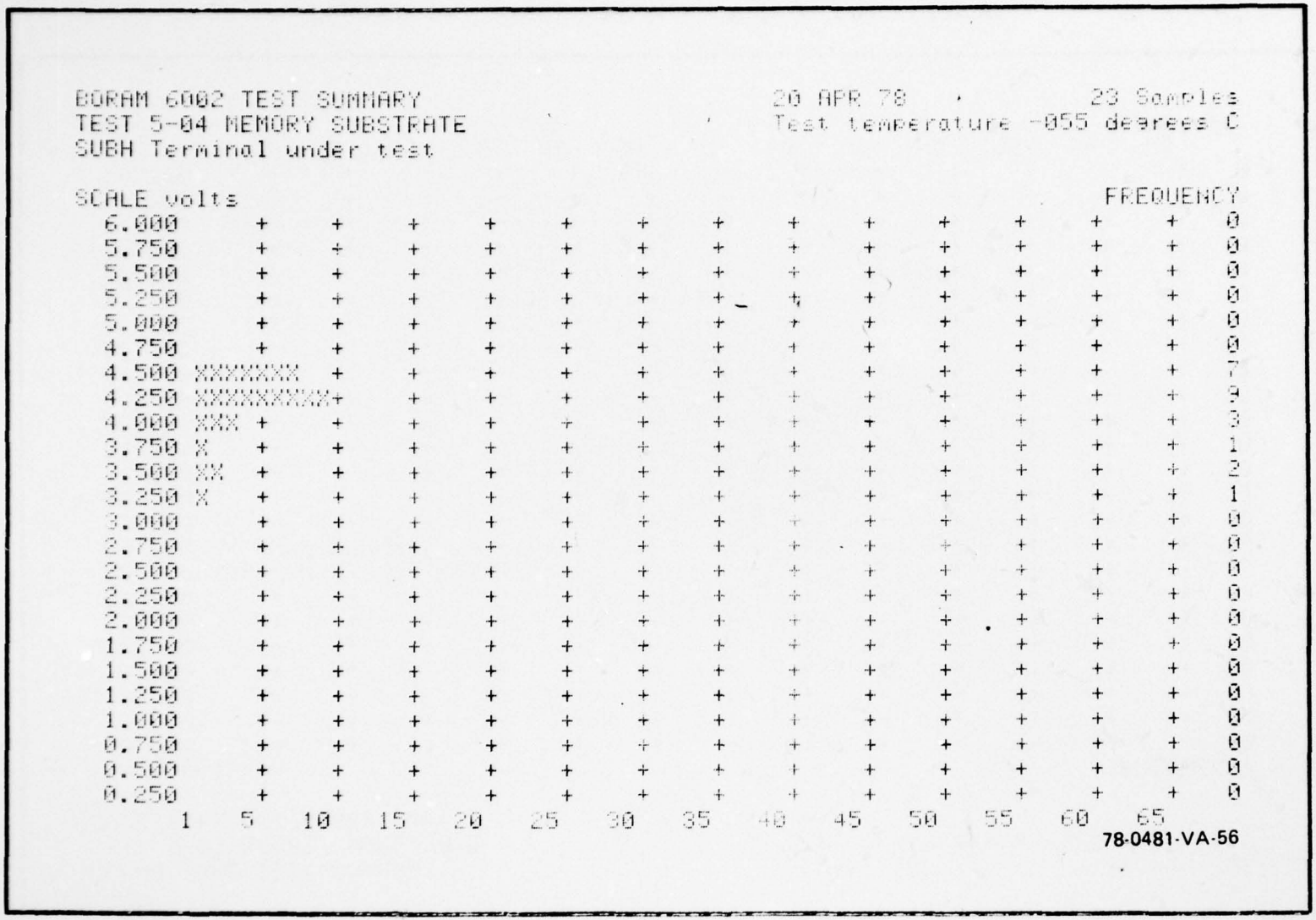

Figure 1-54. Memory Substrate Voltage High at -55°C

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MNOS BORAM MANUFACTURING METHODS AND TECHNOLOGY PROJECT.(U)
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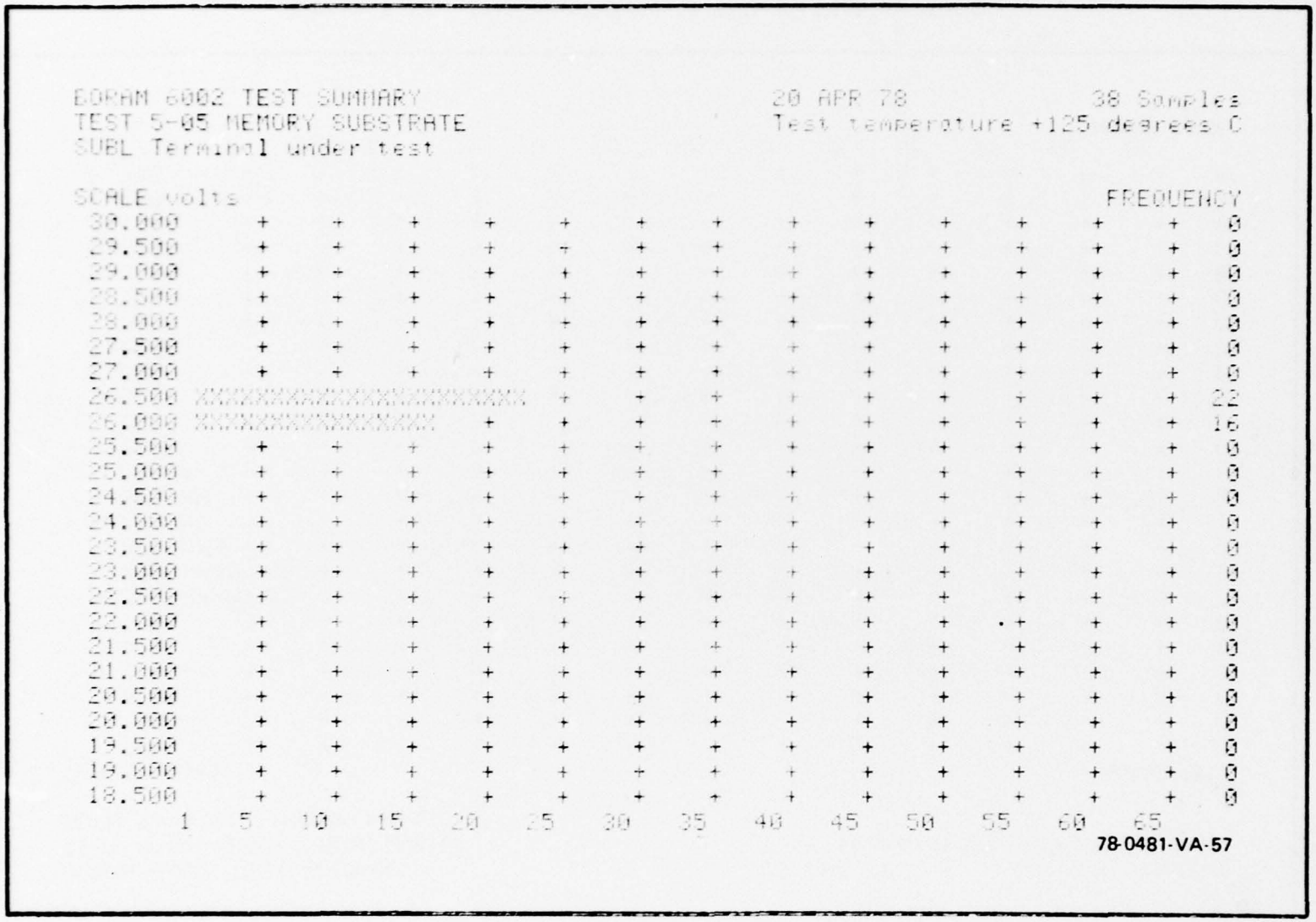

Figure 1-55. Memory Substrate Voltage Low at 125°C

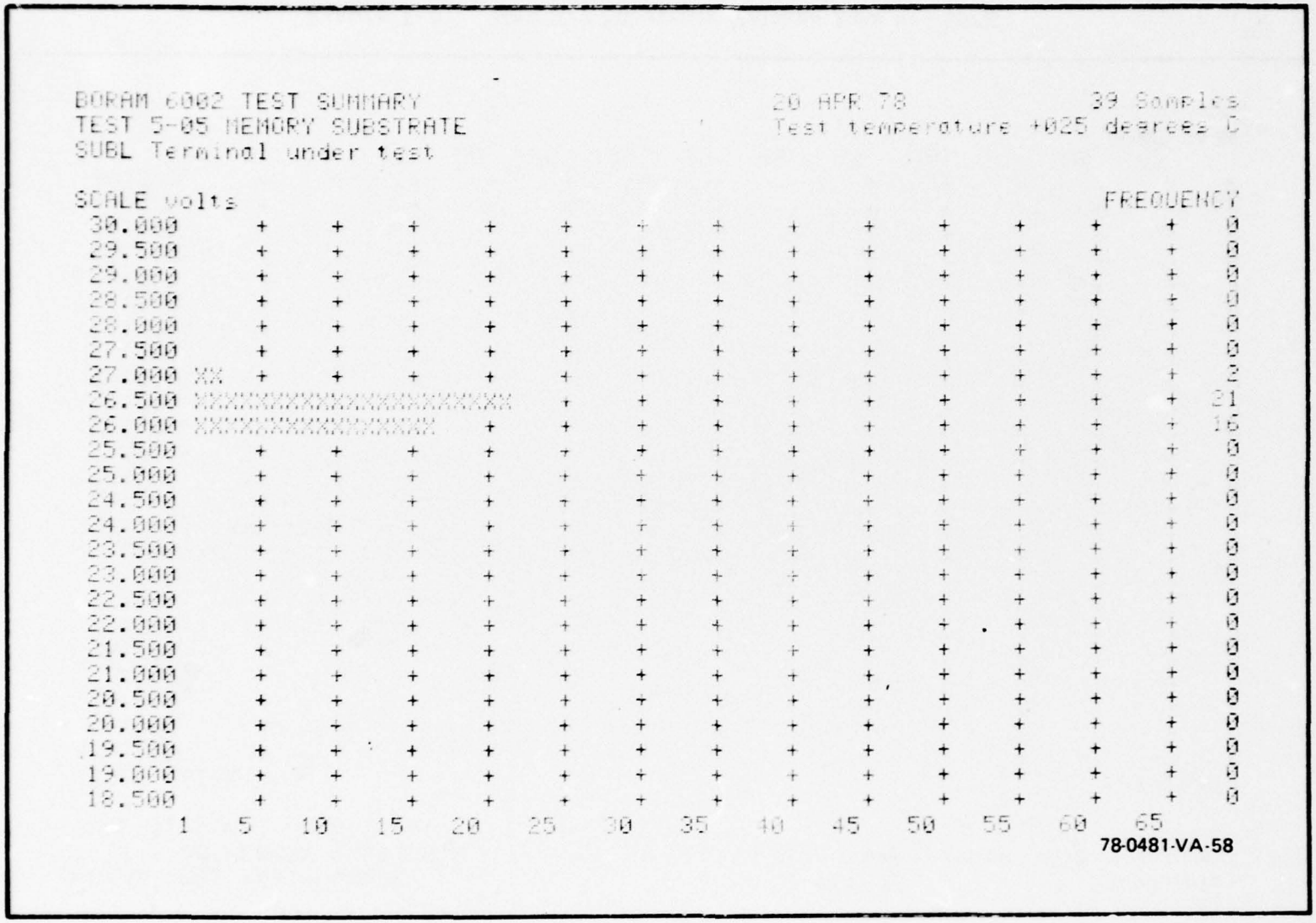

Figure 1-56. Memory Substrate Voltage Low at 25°C

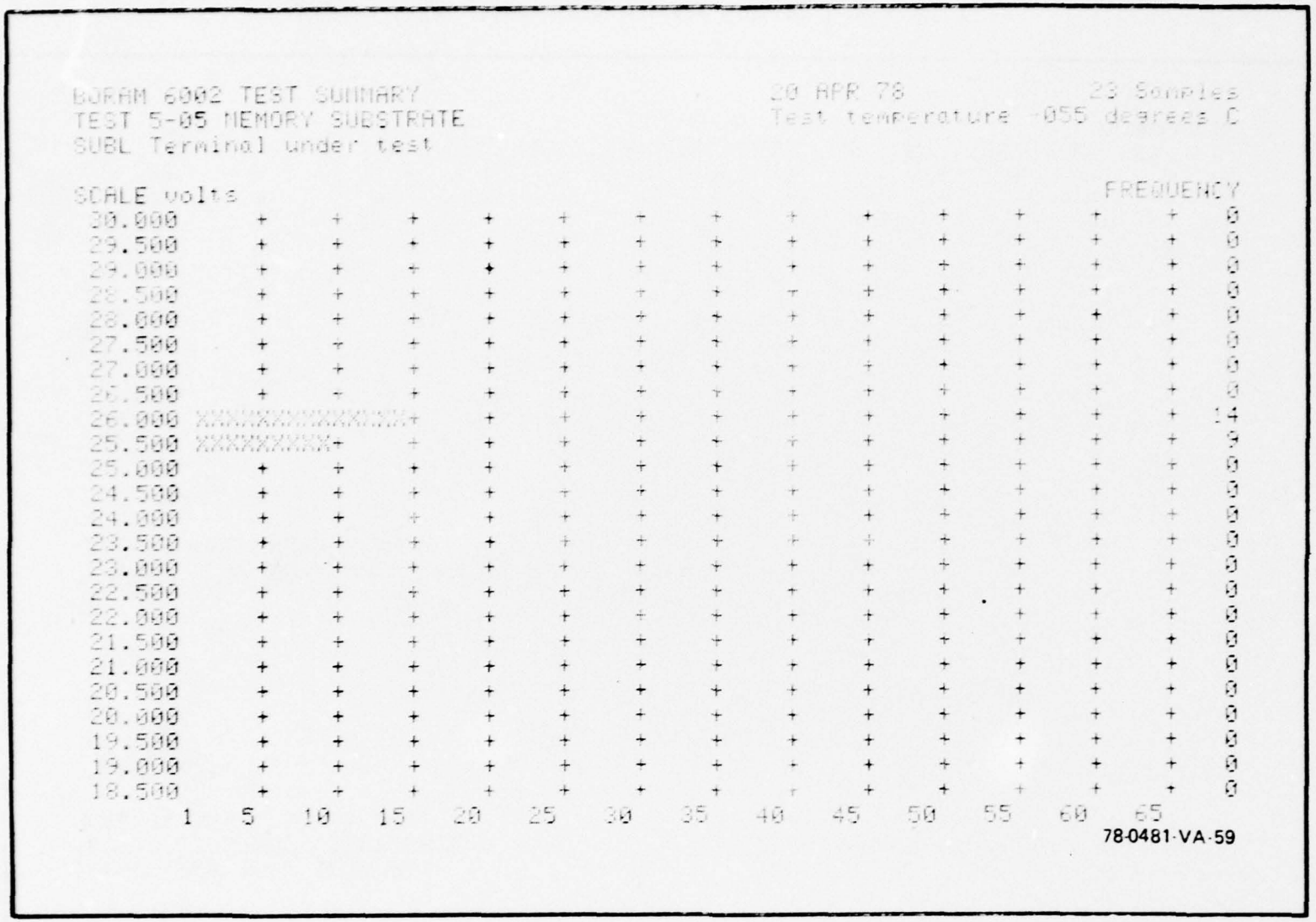

Figure 1-57. Memory Substrate Voltage Low at -55°C

1.5 PRODUCTION ACTIVITY

During the reporting period production learning for the BORAM 6002 chip has continued, and yields have risen significantly. Table 1-24 compares current experience with the initial chip fabrication results.

The MM&T project began work with the 6000C chip, and achieved a yield of about 1.5 die per wafer start. The initial experience with the 6002 chip was about 11 die per two-inch wafer. Current results exceed 33 die per wafer.

Conservative mathematical yield models predict average probe yields of 0.38 for the 6002 chip. Current average experience is 0.22. The highest yield observed was 87 die per wafer, or about 0.45.

TABLE 1-24
BORAM 6002 YIELD GROWTH

Yield Component	Symbol	Yield Experience	
		2nd Quarter 1977	1st Quarter 1978
Process Yield	Y_W	0.63	0.77
Probe Yield	Y_T	0.09	0.22
Overall Yield	Y	0.06	0.17

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2. CONCLUSIONS

The BORAM 6002 chip has been brought to the stage of maturity necessary for low risk manufacture. Production learning trends are firmly established, and costs can be expected to reduce as volume levels increase. All the ground work necessary for pilot production has been completed.

3. PROGRAM FOR NEXT INTERVAL

The primary task during the next period is completion and delivery of the confirmatory sample hybrids, and initiation of the pilot run.

4. PUBLICATIONS AND REPORTS

During the reporting period there were no publications derived directly from this contract effort.

5. IDENTIFICATION OF TECHNICIANS

The following key engineers and management personnel were employed on the BORAM manufacturing methods project from January to March of 1978.

Technician	Manhours
R. Crebs	169
P. Smith	8
C. Waldvogel	8

Mr. K. H. Gibbs has replaced J. L. Hetrick as the program financial manager.

APPENDIX A

TECHNICAL REQUIREMENT SCS-503

Metal Nitride Oxide Semiconductor (MNOS) Integrated Circuits for Block Oriented Random Access Memory (BORAM)

1. SCOPE

1.1 This specification covers the detailed requirements for metal nitride oxide semiconductor integrated circuit chips for use in the manufacture of block oriented random access memory modules.

2. APPLICABLE DOCUMENTS

2.1 The follwing documents of the issue in effect on the date of invitation for bid, form part of this specification to the extent specified herein.

SPECIFICATION

Military

MIL-P-11268	Parts, Materials and Processes Used in Electronic Equipment
MIL-M-38510	Microcircuits, General Specification for

(Copies of documents required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number or symbol should be stipulated when requesting copies.)

3. REQUIREMENTS

3.1 MNOS BORAM Chip Functional Description. The MNOS BORAM chip covered by this specification shall be a 2048 word by 1 bit memory array, and shall have the following features:

- o Nonvolatile electrically alterable memory for implementation of memory systems.
- o 2048 bits organized as 2048 by 1 or 1024 x 2
- o Sequential Input Data Format
- o Internal serial to parallel transfer to provide at least 1.0 MHz data rate with a 26 KHz row decode rate.

- o Block clear of 2048 bits.
- o Data I/O 15 volt CMOS compatible.
- o Address Inputs and Clock Phases 15 volt CMOS compatible.
- o Chip select with P-channel compatible levels.
- o Write and clear address controlled by chip select (CS).
- o Power strobed by chip select to minimize standby power.
- o Output "Tri-state" to permit "wire-or" tie.
- o Memory expansion simplified by chip select logic.
- o Charge enhancement read to extend period of nonvolatile memory.
- o Operating temperature $-55^{o}C$ to $125^{o}C$.

3.2 Physical Characteristics. The BORAM chips shall be fabricated using silicon wafer and P-type metal oxide semiconductor (PMOS) technology in addition to the metal nitride oxide semiconductor (MNOS) techniques. The BORAM chip shall have maximum dimensions of 0.250 inches by 0.250 inches.

3.3 Memory Characteristics. The BORAM chip memory characteristics shall be as follows:

3.3.1 Operation. Operation of the BORAM chip is defined as: the sequencing of controls to clear the chip and write in a digital data sequence, and the sequencing of controls to read out the digital data from the chip and compare it to the input data sequence. Failure of any data bit to compare constitutes failure of operation.

3.3.2 Capacity. The BORAM chip shall have a capacity of 2048 bits of data. This data shall be accessed, for reading or writing, by a serial shift register on the BORAM chip.

3.3.3 Retention. The BORAM chip shall be capable of retaining the data for at least 4000 hours. For purposes of testing this characteristic can be verified by extrapolation.

3.3.4 Electrical Alterable. The BORAM chip shall be capable of being cleared and new data written in and verified electrically.

3.3.5 Read. The BORAM chip shall exhibit no detectable deterioration of signal levels after being read ten times.

3.3.6 Non-Volatile. The BORAM chip shall retain the data upon removal of electric power.

3.4 Chip Select. The BORAM chip shall be so designed that the chip select signal shall enable all other chip functions. Whenever the chip select is a logic zero, the chip with power supplies attached shall draw minimum power and shall be unaffected by any other signals. When the chip select is a logic one the chip shall be active and shall respond to all other signals.

3.5 Electrical Ratings. The BORAM chip shall operate as specified with power supply variations of +1% and signal input variations of +1%.

3.5.1 Power Supplies. The BORAM chip shall have the following power supplies:

VCC	=	+15 volts	(most positive voltage)
CL	=	0 volts	(intermediate negative voltage)
VGG	=	-15 volts	(most negative voltage)

3.5.2 Signals. The electrical signals to the BORAM chip shall be as follows:

3.5.2.1 Signal Descriptions. The signals to the BORAM chip are given in the following subparagraphs.

3.5.2.1.1 Address Lines. The BORAM chip shall have no more than six address lines (A0-A5). These lines shall serve to define the row or data bits to be read or written.

3.5.2.1.2 Access Enable. The access enable (AE) signal shall enable the address select into the memory array area of the chip for purposes of reading or writing data.

3.5.2.1.3 Clocks. The two clock signals (Ø1, Ø2) shall cause the sequencing of the on chip shift register to cause data to be transfered into or out of the chip.

3.5.2.1.4 Clear. The clear signal (CL) shall cause the two transistor cells in the BORAM chip to be reset so that data can be written into the chip.

3.5.2.1.5 Transfer. The transfer signal (TR) shall cause the transfer of data into and cut of the shift register in a parallel form to the memory secton of the chip.

3.5.2.1.6 Memory Write. The memory write signal (MW) shall cause a row of data to be written into memory.

3.5.2.1.7 Data Input. The data input line (DW) shall provide input data to the shift register.

3.5.2.1.8 Data Output. The output line (DR) shall represent the data output of the shift register. Whenever chip select is a logic zero, the output shall be disabled and shall present an impedance greater than 500 ohms.

3.5.2.2 Signal Levels. The voltage levels for logic one and logic zero for the signals to the BORAM chip shall be as follows:

SIGNAL	LOGIC ZERO	LOGIC ONE
Ai/j, $\overline{AE}$, $\overline{TR}$, $\overline{MW}$	VCC - 10.5	VCC - 2.0
Ø1, Ø2	VCC - 14.25	VCC - 2.0
CL	VCC - 14.85	VCC - 2.0
CS	VCC - 34.65	VCC - 2.0
DW	VCC - 10.5	VCC - 2.0
DR	VCC - 10.5	VCC - 4.5

3.6 Electrical Characteristics.

Block Read Cycle Time:	<2.5 msec per 2048 bits
Data Rate:	>1.0 MHz
Memory Clear Pulsewidth:	1000 usec max per write cycle
Memory Write Pulsewidth:	200 usec max
Block Write Cycle Time:	<16 msec per 2048 bits
First Bit Access Time:	<5 usec
Read Mode Power Dissipation:	<670 mW at 25°C
Write Mode Power Dissipation:	<700 mW at 25°C
Standby Power Dissipation:	<1 mW

3.7 Mounting. The BORAM chips shall be mounted in hybrid packages. Sixteen (16) MNOS BORAM IO chips shall be mounted in each hybrid package to permit testing individually or of the entire assembly.

3.8 Environmental Requirements. The MNOS BORAM chip as mounted in the hybrid package shall comply with the requirement of paragraph 3 and in particular operation as defined in 3.3.1, of this specification after being subjected to mechanical shock, vibration, constant acceleration and high temperature environments. (See 4.5 Tables 1 and 2).

3.9 Process Conditions. All units shall be process conditioned. (see table 1).

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection. Unless otherwise specified in the contract or purchase order, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract or order, the supplier may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in the specification where such in spections are deemed necessary to assure supplies and services conform to prosecribed requirements.

4.2 Classification of Inspection. Inspection shall be classified as follows:

(a) First Article inspection (does not include preparation for delivery (see 4.3).

(b) Quality conformance inspection (see 4.4)

4.2.1 Process Conditioning. Confirmatory sample units shall be process conditioned per Table 1. Pilot run units do not require stabilization bake and temperature cycle, but shall otherwise be conditioned per Table 1. Subsequent production shall be conditioned per Table 1.

4.3 Confirmatory Sample Inspection. Confirmatory sample testing shall consist of the tests specified in Table 2. All confirmatory sample units shall be subjected to these tests.

4.4 Quality Conformance Inspection. The contractor is not required to perform a Quality Conformance inspection on pilot run production. Subsequent production shall be inspected per Table 2.

4.5 Test Plan. The contractor prepared, Government - approved test plan shall contain:

(a) An operational test method to show that the BORAM chips as mounted in hybrid packages, satisfactorily meet the requirements of paragraph 3, and in particular operation as defined in paragraph 3.3.1.

(b) Time schedule and sequence of examinations and tests.

(c) A description of the method and procedures.

(d) Program of any automatic tests including flow charts and block diagrams.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery shall be in accordance with the best commercial practice.

TABLE 1 PROCESS CONDITIONING REQUIREMENTS

Conditioning Operations	MIL-STD 883 Test Method	Description
Stabilization Bake	1008.1 Condition C	24 hour bake at 150°C with no end point measurements.
Temperature Cycle	1010.1 Condition B	10 cycles required with no end point measurements.
Pre Burn-In 25°C Electrical Test	Does Not Apply	Test must conform to SC5-503 paragraphs 3 and 4.5.
Burn-In Test 125°C Ambient	1015.1 Condition C	Steady-state, power and reverse bias for 160 hours.
Post Burn-In 25°C, 125°C, -55°C Electrical Tests	Does not Apply	Tests must conform to paragraphs 3 and 4.5. of SCS-503.

TABLE 2 GROUP C TESTS (NOTE 1)

EXAMINATION OR TEST	MIL-STD 883 TEST METHOD	FAILURES ALLOWED
Subgroup 1		
Mechanical Shock	2002 Condition B	1
Variable Vibration	2007 Condition A	1
Constant Acceleration	2001 Condition B	1
Subgroup 2		
High Temperature Storage	1008 Condition C	0

NOTE 1 - End point electrical tests are required after each test per method specified in paragraph 4.5.

APPENDIX B

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Addressee	Qty
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